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Impact of Structural and Doping Parameter Variations on NQS Delay, Intrinsic Gain and NF in FinFETs

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***Abstract*— This paper investigates the effect of process variations on RF metrices, non-quasi static (NQS) delay, intrinsic gain and noise figure (NF) in 30 nm gate length FinFET by performing extensive 3D TCAD simulations. Sensitivity of NQS delay, intrinsic gain and NF on different geometrical parameters, channel doping, source/drain doping are studied. The most significant parameters are found to be gate length, underlap, oxide thickness, fin width and height, source/drain doping.**

***Index Terms*—** FinFET, NQS delay, intrinsic gain, NF, TCAD

I. INTRODUCTION

Multi-gate devices are thought as a potential alternative to MOSFETs. Even though initially, many double gate devices were suggested in the area of multi-gate transistors, double gate FinFETs are considered as a serious contender for channel scaling. Because of their quasi-planar structure they are compatible with the existing CMOS technology. Since, these devices use ultrathin bodies as their channel, suppression of short channel effects (SCEs) can be achieved with undoped channels instead of the usual high doping density channels. Abundant literature was available on FinFETs [1-4].

FinFET-based analog building blocks/RF receivers have been investigated extensively [5, 6]. RF performance of FinFETs is studied [7-9]. In the above mentioned literature, the effect of fin width on unity gain cut-off frequency (f_t) and maximum frequency of oscillation (f_{max}) has been investigated. The source/drain series resistance in FinFETs largely limits the device RF performance, and the losses due to the gate resistance increases with reducing gate length. Nuttinck et al [10] has studied about the source/drain resistance impact on RF performance

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In this paper, nine different geometrical parameters and two doping related parameters of FinFET are varied over a wide range to study their effect on NQS delay, intrinsic gain and noise figure. Next section describes the simulation environment. Section III discusses the simulation results. Finally section IV we provides conclusions.

II. Simulation Environment

2.1 Device Description

Sentaurus TCAD simulator from Synopsys [11] is used for this study. Figure 1 shows the 2D structure of the FinFET. The 3D device structure is shown in Figure 2(a). Figure 2(b) shows a 2D cut of the above 3D structure which depicts the fin cross section i.e. in Fig. 2(b) source to drain axis runs perpendicular to the page.

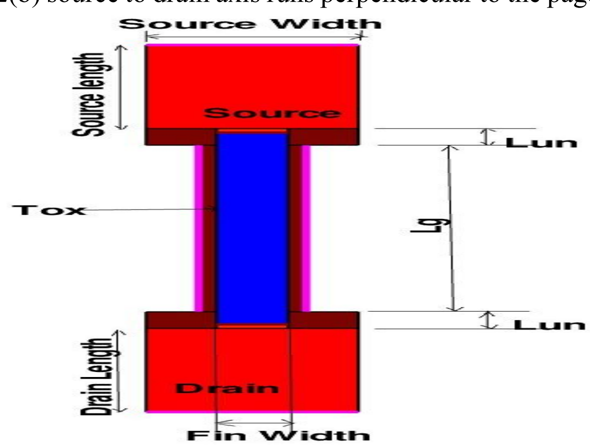


Figure 1: 2D structure of FinFET

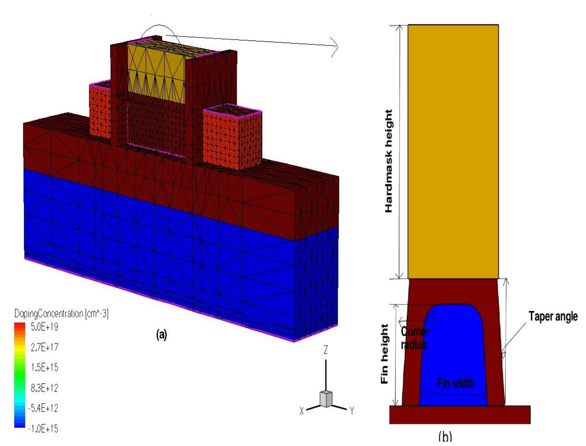


Figure 2: (a) 3D structure of FinFET (b) Enlarged portion of the rounded region

2.2 Parameter Space

The effect of process parameters, gate length (L_g), underlap (L_{un}), fin width (W), gate oxide thickness (T_{ox}), channel doping (N_{ch}), and source/drain doping (N_{SD}) on NQS delay, intrinsic gain and NF are studied with the 2D simulations. Some of the parameters like fin height (H), source/drain cross-sectional area, fin taper angle, corner radius and hard mask height (HM) cannot be studied with 2D simulations. So these parameters are studied with 3D simulations.

Device simulator includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. The simulator was calibrated against the published results on FinFETs [12]. After calibration, the device dimensions are brought to the requirements as given in Table 1. Table 1 gives the dimensions of the nominal device and also tells the range for the various parameters studied in this paper

Table 1: Dimensions of the nominal device and their range of values in FinFETs

Process parameters	Nominal value	Range of values
Gate length (L_g)	30 nm	20 nm - 40 nm
Fin width (W)	4 nm	3 nm - 10 nm
Fin height (H)	4 nm	2 nm -7 nm
Underlap (L_{un})	3 nm	1 nm - 8 nm
Source/Drain cross sectional area	22.5 nm^2	16 nm^2 - 48 nm^2
Oxide thickness (T_{ox})	1 nm	0.5 nm - 3 nm
Fin-taper angle	2 ^{o}	0^o - 5^o
Corner radius	1 nm	0 nm - 2 nm
Hard mask height (HM)	10 nm	0 nm- 100 nm
Channel doping (N_{ch})	1X10^{16}/cm^3	1X10^{15}/cm^3-1X10^{19}/cm^3
Source/drain doping (N_{SD})	1X10^{20}/cm^3	1X10^{18}/cm^3-2X10^{20}/cm^3

2.3 Simulation Methodology

The RF non-quasi-static delay in the devices is studied using transient simulation. To evaluate the small signal response, a small time varying ac signal along with a DC bias is applied to the gate. The delay between the applied gate signal and drain current is measured to get the NQS delay. The intrinsic gain can be defined as the product of trans-conductance (g_m) and output resistance (R_o). Noise simulation in SDEVICE is a standard AC simulation with noise models included in the physics section. The results from the noise simulation are used to extract the noise figure which is given by

$$NF = 1+\frac{1}{S_I^s}\left\{S_I^{gg} + |\alpha|^2 S_I^{dd} - 2\,\mathrm{Re}(\alpha S_I^{gd})\right\} \quad (1)$$

$$\alpha = \frac{Y_s + Y_{11}}{Y_{21}} \quad (2)$$

S_S^I is the current noise spectrum of the noisy source admittance and is given by

$$S_S^I = 4k_B T\,\mathrm{Re}(Y_S)$$

S_I^{gg} and S_I^{dd} are the noise current spectrums, at the gate and drain terminals respectively, S_I^{dg} is the cross-correlation noise spectra between the drain and gate terminals, Y_{11} (i.e. Y_{gg}) and Y_{21} (i.e. Y_{dg})are the respective admittance parameters.

III. Results and Discussion

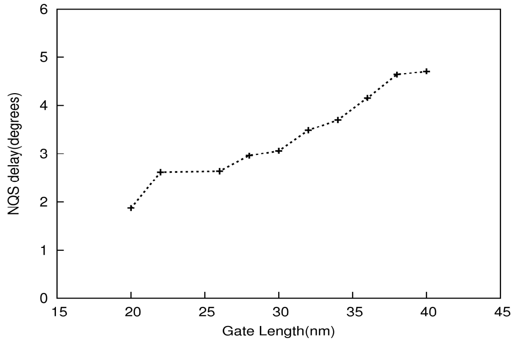
3.1 Impact on NQS Delay

The eleven different process parameters are varied one at a time, according to the range given in Table 1 and their impact on NQS delay is studied in this section. NQS delay is extracted as discussed in Section 2.3 at a frequency of 200 GHz. To reason out the simulation result, the expression given by Allen et al [13] is used. For a particular NQS delay, the NQS frequency (f_{NQS}) is given by

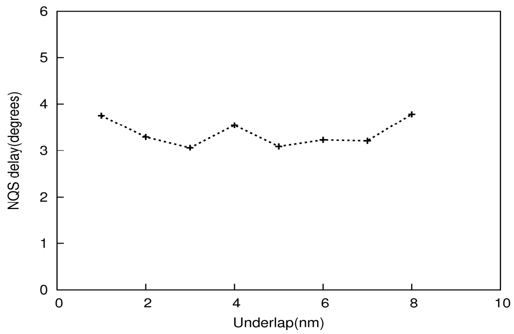
$$f_{NQS} = \frac{\alpha \mu_{eff}(V_{GS} - V_T)}{2\pi L_g^2} \quad (3)$$

where α is the fitting parameter depending on the accuracy required for the simulation to an NQS event, μ_{eff} the mobility, V_{GS} the gate bias and V_T the threshold voltage of the transistor.

Figure 3 show the variation of NQS delay (extracted at 200 GHz) with respect to various parameters. Figure 3 (a) shows the variation of NQS delay with respect to L_g. It can be seen that the delay increases with respect to L_g. Equation 3 predicts that as L_g increases f_{NQS} decreases i.e. for the given frequency NQS delay increases. Figure 3(b) shows the variation of NQS delay with respect to L_{un}. It can be observed that the delay increases as we move from nominal L_{un}. Delay is less significant with respect to oxide thickness, fin width and height. For all other geometrical parameters, NQS delay is the least significant. Delay increases after 1X10^{18}/cm^3 for channel doping whereas it shows a decreasing trend for source drain doping.


NQS delay(degrees)
Gate Length(nm)
15 20 25 30 35 40 45
0 1 2 3 4 5 6

(a)


NQS delay(degrees)
Underlap(nm)
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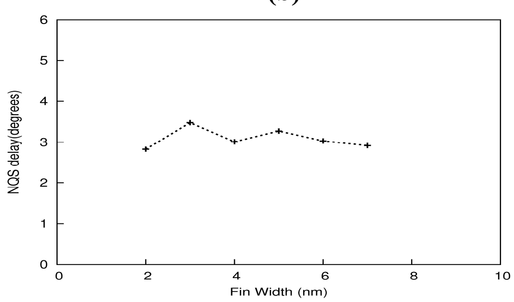
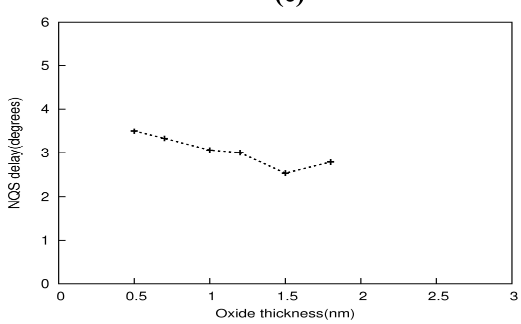
0 1 2 3 4 5 6

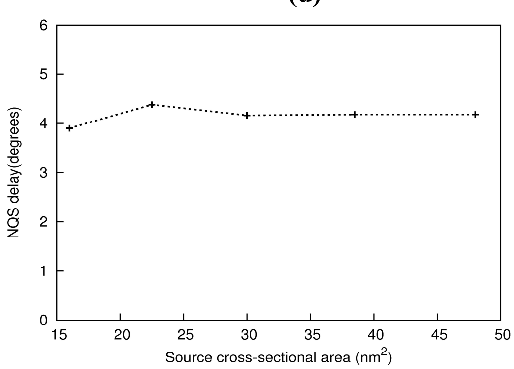
(b)


NQS delay(degrees)
Fin Width (nm)
0 2 4 6 8 10
0 1 2 3 4 5 6

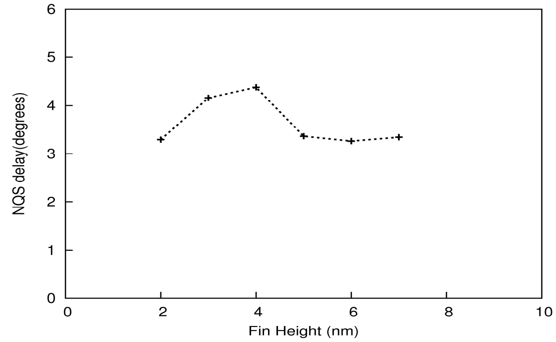
(c)


NQS delay(degrees)
Oxide thickness(nm)
0 0.5 1 1.5 2 2.5 3
0 1 2 3 4 5 6

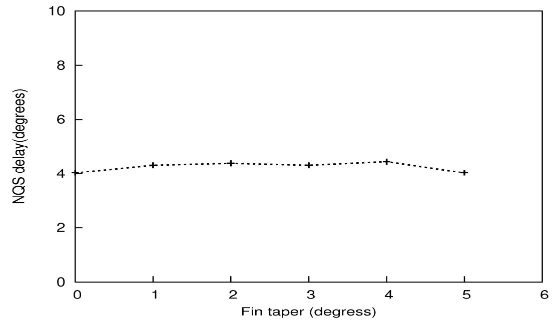
(d)


NQS delay(degrees)
Source cross-sectional area (nm2)
15 20 25 30 35 40 45 50
0 1 2 3 4 5 6

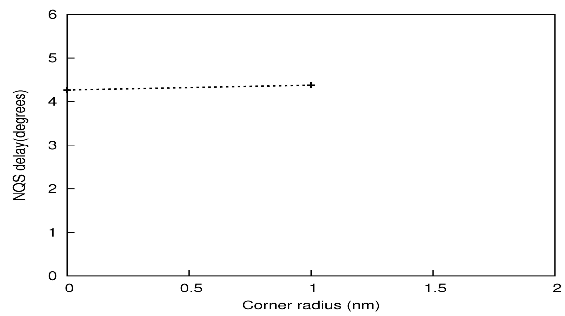
(e)


NQS delay(degrees)
Fin Height (nm)
0 2 4 6 8 10
0 1 2 3 4 5 6

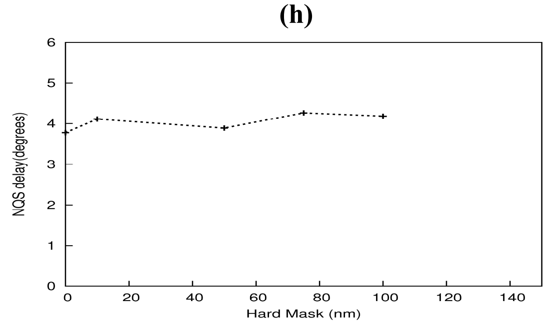
(f)


NQS delay(degrees)
Fin taper (degress)
0 1 2 3 4 5 6
0 2 4 6 8 10

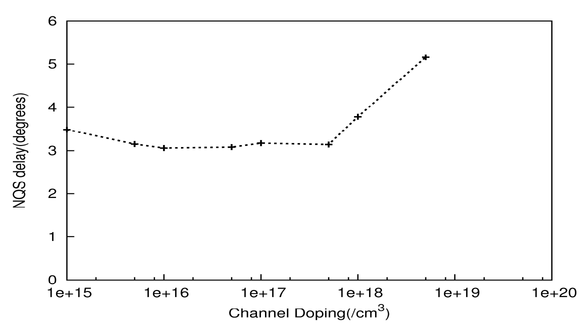
(g)


NQS delay(degrees)
Corner radius (nm)
0 0.5 1 1.5 2
0 1 2 3 4 5 6

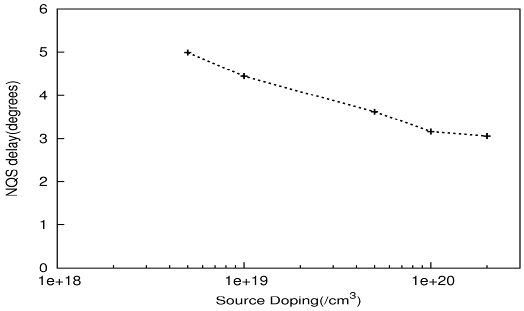
(h)


NQS delay(degrees)
Hard Mask (nm)
0 20 40 60 80 100 120 140
0 1 2 3 4 5 6

(i)


NQS delay(degrees)
Channel Doping(/cm3)
1e+15 1e+16 1e+17 1e+18 1e+19 1e+20
0 1 2 3 4 5 6

(j)

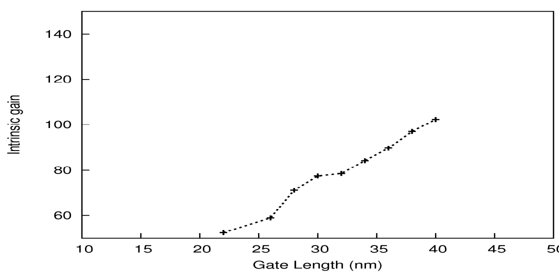


(k)

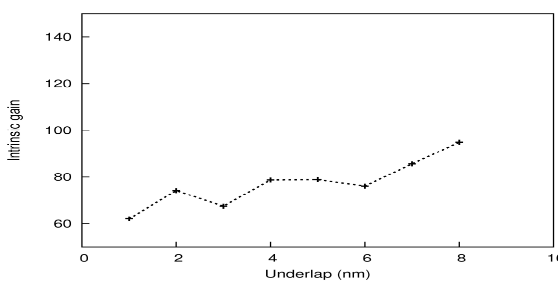
Figure 3: (a)-(k) NQS delay versus structural and doping parameters

3.2 Impact on intrinsic gain

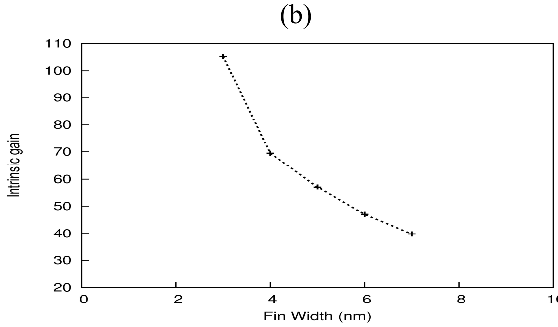
The different structural and doping related parameters are varied one at a time, according to the range given in Table 1 and their impact on intrinsic gain is studied in this section. Since intrinsic gain depends on both g_m and R_o their combined behavior brings the increasing or decreasing tendency with respect to the parameter variation. In the studied region, R_o dominates and decides the trends seen in the Fig. 4. For all the process parameters except source/drain cross sectional area, fin taper, corner radius and hard mask height, intrinsic gain affects significantly.



(a)



(b)



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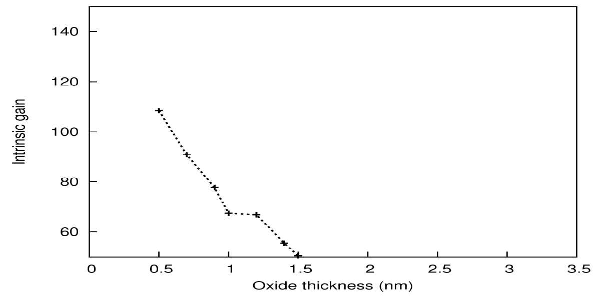

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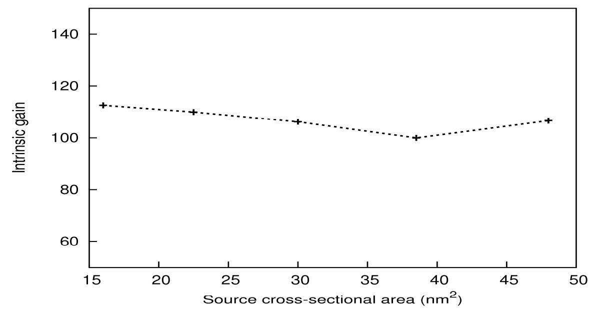

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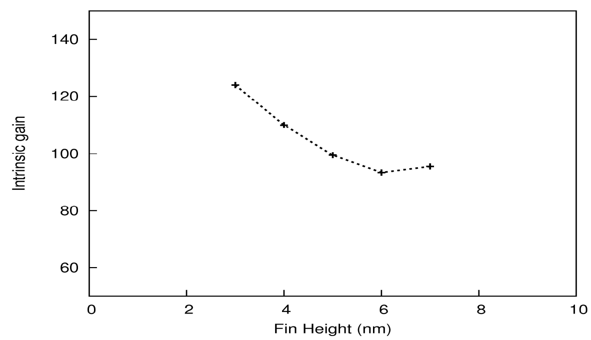

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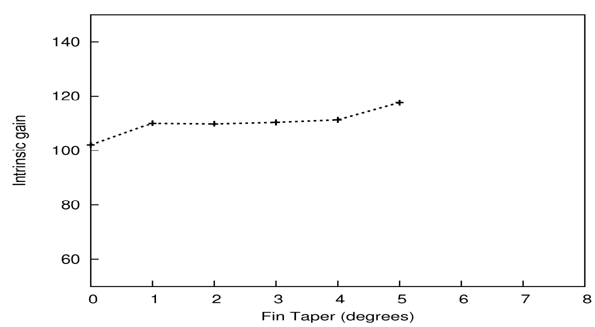

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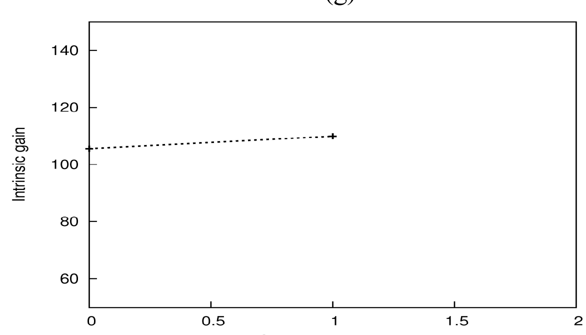

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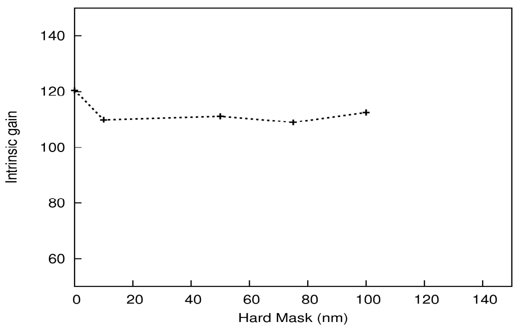

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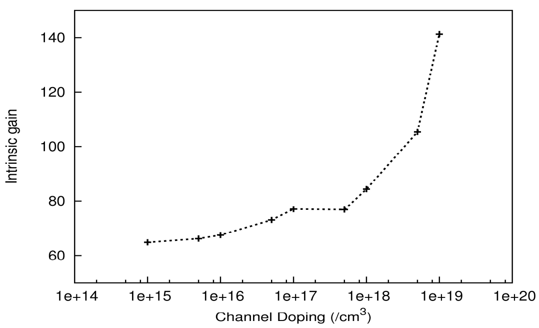

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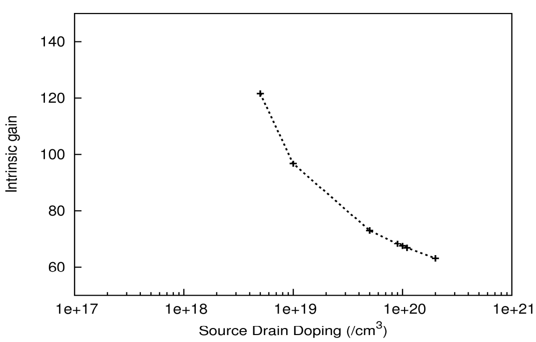


(k)

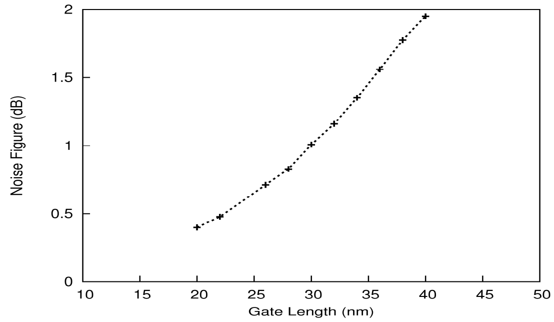
Figure 4: (a)-(k) Intrinsic gain versus structural and doping parameters

3.3 Impact on Noise figure

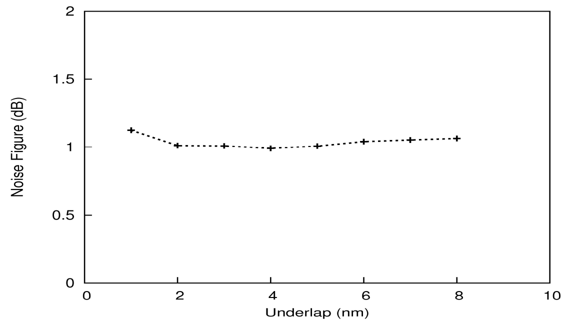
In this section the parameters are varied one at a time, according to the range given in Table 1 and their impact on noise figure is analyzed. NF is extracted using the Equation 1 as discussed in Section 2.3, at a frequency of 10 GHz. The results can be reasoned out using the following expression which relates the noise figure and f_t.

$$NF = 1 + \left(\frac{f_0}{f_t}\right)K \qquad (4)$$

where f_o is the resonant frequency, f_t is the unity gain frequency and K is the noise factor scaling coefficient. It can be observed from Equation 4 that NF is inversely proportional to f_t and so the trends of various parameters with respect to noise figure. This can be evidently seen from our previous results [14]



(a)



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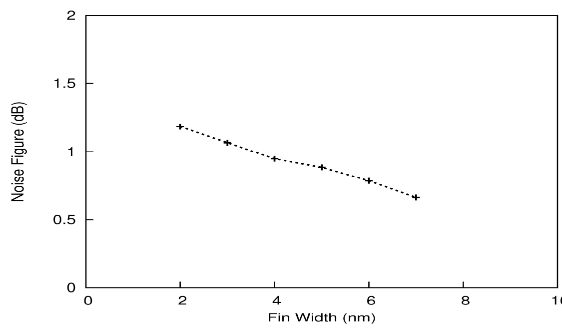

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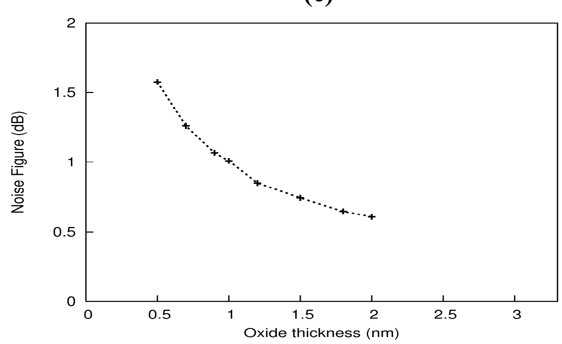

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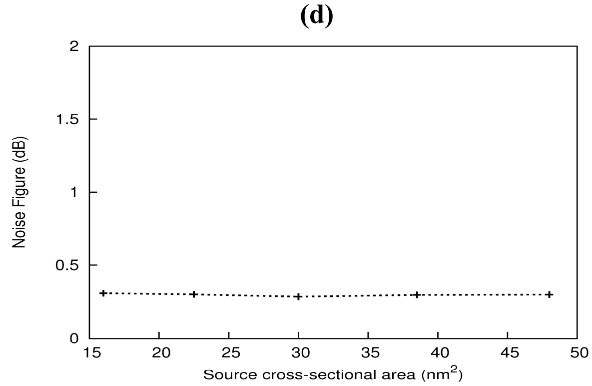

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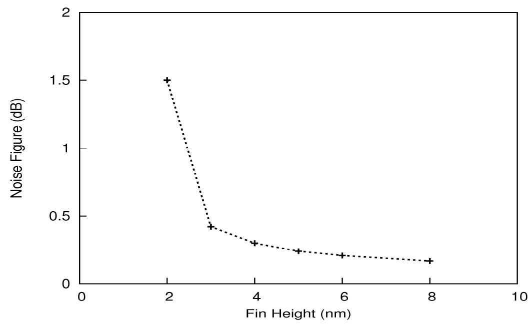

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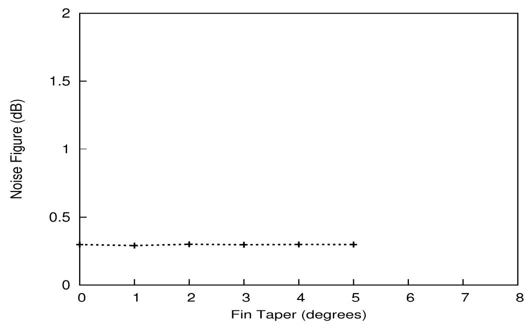

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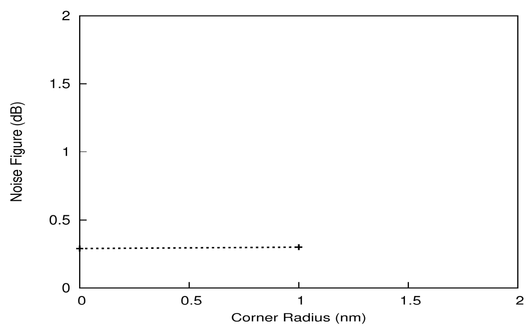

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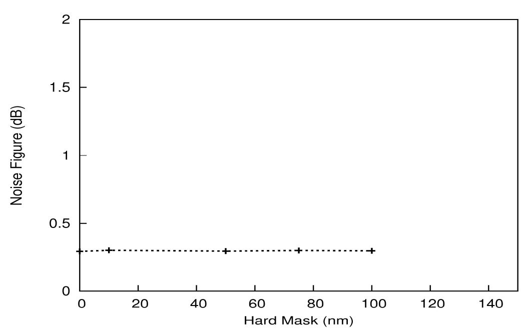

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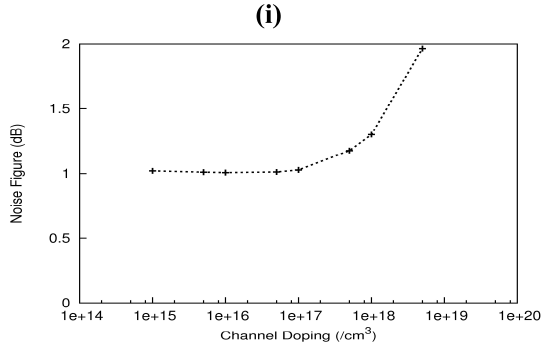

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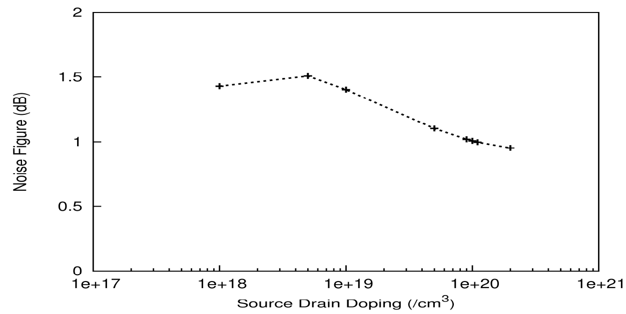

(k)

Figure 5: (a)-(k) Noise figure versus structural and doping parameters

Conclusion

In this paper, the conventional FinFET device is studied for structural and doping parameter variation. Nine structural and two doping parameters are taken as input and their effect on NQS delay, intrinsic gain and noise figure have been studied. The inputs are varied over a wide range to understand the general behavior. It has been found that gate length, underlap, oxide thickness, fin height and width, and source drain doping were the most significant parameters with respect to NQS delay, intrinsic gain and NF. The least significant parameters are source/drain cross sectional area, fin taper, corner radius and hard mask height and channel doping.

Acknowledgement

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