Implementation of Low Power Turbo Encoder and Decoder in Wireless Applications

T. Chandini, V. Jayachandra Naidu

Abstract— **Turbo coding is an advanced forward error correction algorithm in which the encoder generates a data stream consisting of two independently encoded data streams and a single un encoded data stream. The two parity streams are weakly correlated due to the interleaving. It is a standard component in third generation (3G) wireless communication systems, like those employing Wideband Code Division Multiple Access (W-CDMA). W-CDMA systems must handle online multimedia applications as well as conventional voice communications. In the turbo decoder, the two parity streams are separately decoded with soft decision outputs, referred to as extrinsic information. The strength of the turbo decoding results from the sharing of the extrinsic information in a number of iterations. The extrinsic information is passed from one parity decoding step to the other, from one iteration to the other. In this paper, we decompose low complexity turbo decoder architecture by using SB/DB mode algorithm. The proposed architecture is simulated in Cadence encounter (R) RTL compiler and also in Xilinx ISE 14.3 and the power consumption was found to be of 0.0034mW as compared to the existing architecture which consumes a power of 4.17mW.**

Index Terms— Decoder, Encoder, Error Correcting Code, Interleaver and Turbo codes

I. INTRODUCTION

Turbo codes constitute major development in the field of Forward Error Correction (FEC).In electrical engineering and digital communications turbo codes are a class of high performance error correction codes which are essential in deep satellite communication and other applications where designers seek to achieve maximal information transfer over a limited bandwidth communication link in the presence of data corrupting noise. Exhibiting performance approaching the Shannon limit, Turbo Codes (TC) have the TC block set features efficient encoder and decoder designs seen rapid

adoption in the design of digital communication systems. Through the application of systemic design methodology that considers data transfer and storage stop priority candidates for optimization, the author's show how turbo codes can be implemented and the attractive performance results that can be achieved in throughput, latency. This represents a significant development in the field of error-correcting codes. The principle of decoding is to be found in an iterative exchange of information between elementary decoders, called extrinsic information, and it is this principle from which the term turbo originates. The turbo concept is now applied to block codes as well as other parts of a digital transmission system, such as detection, demodulation. Applications that integrate turbo codes into their standards are mobile communications, wireless networks and local radio loops. Future applications could include cable transmission, short-distance communication or scalable transmission, short-distance communication or data storage.

The outline of the work is as follows. Section II discusses about the theory related to turbo codes. Section III discusses about the proposed architecture and Section IV presents design of various sub-blocks associated with the encoder and decoder and its results. Section V is conclusion.

II. Turbo COdes

In information theory, turbo codes (originally in French Turbo codes) are a class of high-performance forward error correction (FEC) codes developed in 1993, which were the first practical codes to closely approach the channel capacity, a theoretical maximum for the code rate at which reliable communication is still possible given a specific noise level. Turbo codes are finding use in 3G mobile communications and deep space satellite communications as well as other applications where designers seek to achieve reliable information transfer over bandwidth- or latency-constrained communication links in the presence of data-corrupting noise. Turbo codes are

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nowadays competing with LDPC codes, which provide similar performance.

With rapid growth of multimedia services, the Convolutional turbo code (CTC) has been widely adopted as one of forward error correcting (FEC) schemes of wireless standards to have a reliable transmission over noisy channels. Single-binary (SB)CTC, proposed in 1993 , has been the well-known FEC code that can achieve high data rates and coding gains close to the Shannon limit. The SB CTC code has been adopted in the FEC schemes of wideband code division multiple access (WCDMA), high speed downlink packet access (HSDPA), and long term evolution (LTE) [1]-[2]. In 1999, non-binary CTC was introduced to achieve superior performance than the SB CTC. In recent years, double-binary (DB) CTC has been adopted in advanced wireless communication standards, such as worldwide interoperability for microwave access (Wi-MAX). Some CTC decoders have been implemented as application-specific integrated circuits (ASICs), such as the HSDPA CTC decoder and Wi-MAX CTC decoder. Recently, high-end portable/mobile devices become prevalent in wireless markets. There are large growing emergence and demands for an inexpensive solution to access the ubiquitous wireless services. Meanwhile, these wireless standards, such as 3GPP and Wi-MAX standards, adopted CTC schemes with different coding parameters and different throughput rates. To deal with the accelerated evolution of these standards, the multi standard platforms which can seamlessly work across the multiple standards were proposed in. Hence, a CTC decoding accelerator which works in the multi standard platforms is desired to achieve the smooth migration for the multiple wireless applications.

Reliable data transmission in wireless communication systems requires sophisticated channel coding schemes and corresponding high-throughput, low area, and energy-efficient decoder implementations. Convolutional codes (CCs) used in stand-alone form or as part of turbo codes , are among the most popular codes used in current and next-generation wireless communication standards, such as HSDPA , 3GPP-LTE , LTE-Advanced , or IEEE 802.11n . CCs and turbo codes are of significant practical interest due to the fact that they offer excellent error-correction performance and can be implemented to achieve high throughput, while being efficient in terms of silicon area and power consumption. Since the advent of turbo codes, iterative decoding algorithms relying on CCs, became a key enabler for wireless communication systems operating close to the Shannon limit. CCs have also been considered for wireless communication systems employing iterative detection and decoding, i.e., where reliability information is exchanged iteratively between a detector and the channel decoder. In particular, iterative detection and decoding in multiple-input multiple-output (MIMO) wireless systems or systems exhibiting inter-symbol interference is becoming an integral part of future transceiver designs because it is an efficient means to substantially improve the throughput and quality-of service (i.e., link reliability, coverage, and range) compared to non-iterative decoding schemes.

III. proposed system architecture

Figure 1 shows the block diagram for generation of SB/DB Modes by Turbo encoder.

1.1 Turbo encoder structure

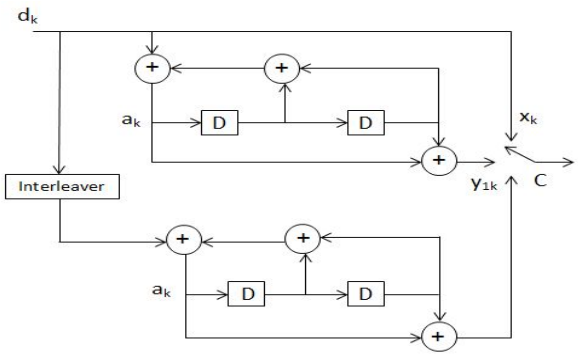

Fig. 1. Block diagram for generation of SB/DB Modes by Turbo encoder

As shown in Fig. 1, the Turbo encoding scheme in the LTE standard is a parallel concatenated convolutional code with two 8-state constituent encoders and one convolutional interleaver [5]. The function of the convolutional interleaver is to take a block of N-bit data and produce a permutation of the input data block. From the coding theory perspective, the performance of a Turbo code depends critically on the interleaver structure [8]. The basic LTE Turbo coding rate is 1/3. It encodes an N-bit information data block in to a code word with 3N+12 data bits, where 12 tail bits are used for trellis termination. The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input information bits. LTE has defined 188 different block sizes.

The convolutional encoder can be represented as follows [6]:

- $g_0 = 1 + D + D_2 + D_3 + D_6$
- $g_1 = 1 + D_2 + D_3 + D_5 + D_6$

The convolutional encoder basically multiplies the generator

Polynomials by the input bit string, as follows:

- $A(x) = g_0(x) * I(x) = a\ b\ c\ \ldots\ g$
- $B(x) = g_1(x) * I(x) = P\ Q\ R\ \ldots\ V$

Interleaving the two outputs from the convolutional encoder yields $E(x) = aPbQcR\ldots gV$, which can also be written as:

$E(x) = (a_0\, b_0\, c_0 \ldots g_0) + (0P0Q0R \ldots 0V) = A(x2) + x*B(x2)$

Therefore, $E(x) = A(x2) + x*B(x2)$ and $A(x2) = g0(x2) + I(x2)$ and $B(x2) = g1(x2) * I(x2)$, with the following:

$E(x) = g0(x2) * I(x2) + x * g1(x2) * I(x2)$

$= I(x2) * (g0(x2) + x * g1(x2))$

$= I(x2) * G(x)$

Where $G(x) = g0(x2) + x * g1(x2)$

i.e. $G(x) = 1 + x + x2 + x4 + x5 + x6 + x7 + x11 + x12 + x13.$

3.2 Decoder Structure

The general scheme of a basic decoder is shown in Figure 2. Two component decoders are linked by two interleavers and two de-interleavers. Each component decoder has three inputs: the systematic information, the parity information, and the information from the other component decoder. This information from the other decoder is referred to as a priori information. Both component decoders have to process both the inputs from the channel as well as a priori information from each other.

Normally used component decoders are having more complexity and architecture. So to reduce the architecture the component decoders are implemented with the normal decoding architecture. Figure 2 shows the block diagram of Turbo Decoder using SB/DB Mode

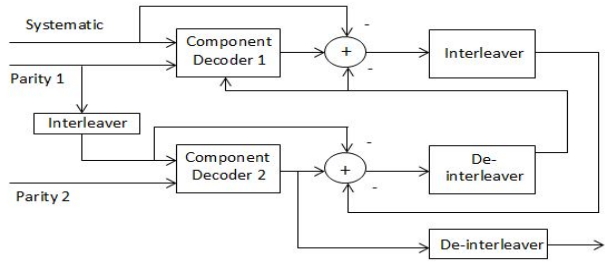

Figure 2 Block diagram of Turbo Decoder using SB/DB Modes

IV. Results and discussions

The proposed architecture is simulated in Cadence encounter (R) RTL compiler and also in Xilinx ISE 14.3. Figure 3 shows the RTL schematic of turbo encode

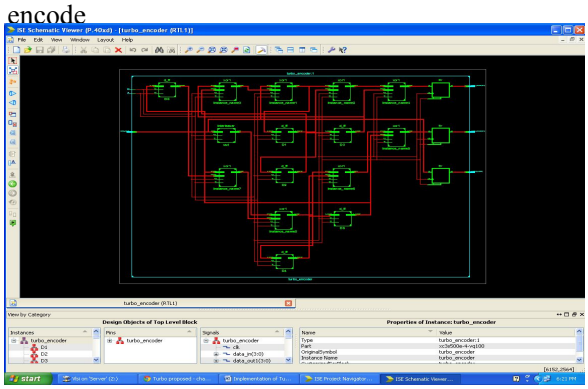

Fig 3 RTL Schematic diagram of Turbo encoder

Figure 4 shows the technology schematic of Turbo Encoder.

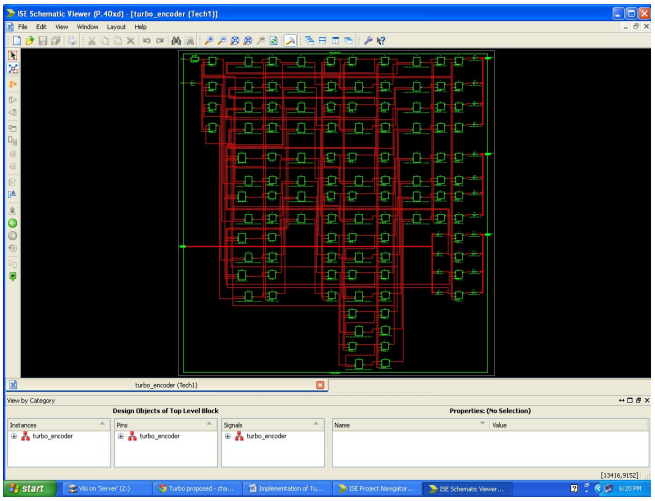

Fig .4 Technology Schematic diagram of Turbo Encoder

Figure 5 shows the RTL Schematic of Turbo Decoder.

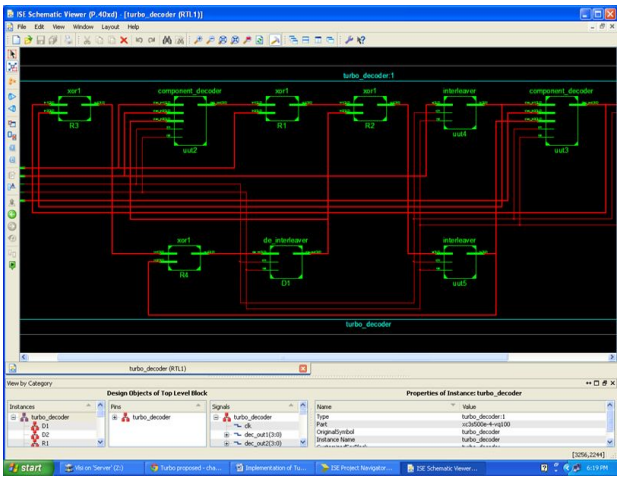

Fig.5. shows the RTL Schematic of Turbo Decoder

Figure 6 shows technology schematic of Turbo Decoder.

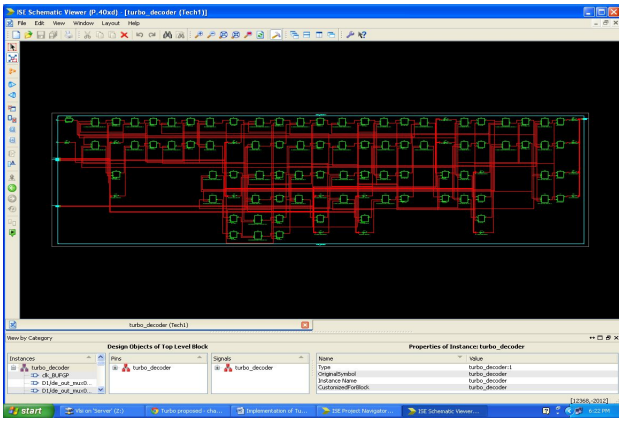

Fig.6. Technology schematic diagram of Turbo Decoder

Figure 7 shows the technology schematic of Top Module.

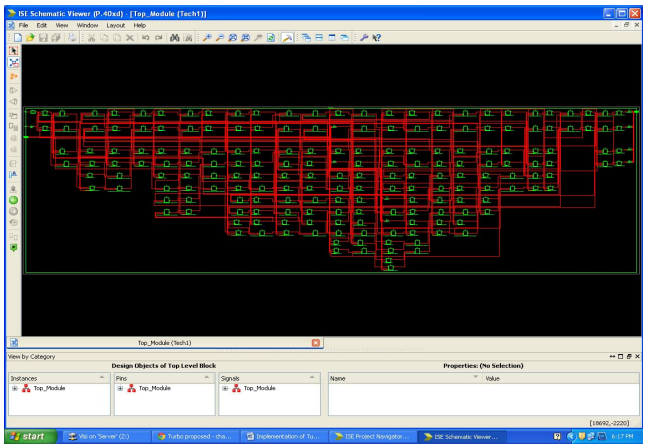

Fig.7. Technology schematic of Top Module

Figure 8 shows the RTL schematic of Top Module.

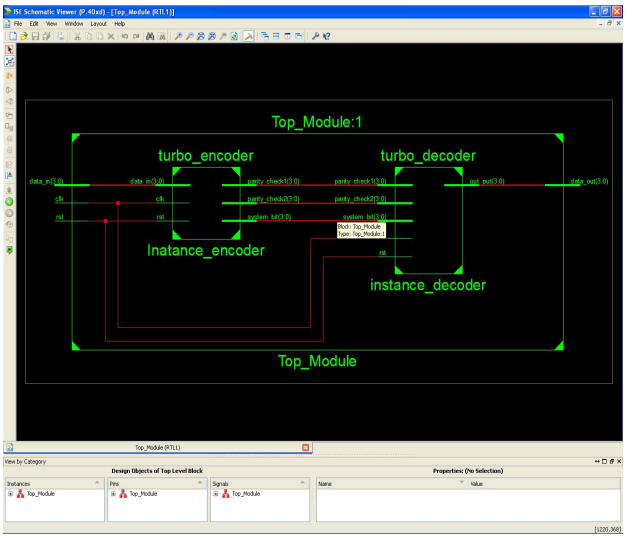

Fig.8. RTL schematic diagram of Top Module

Figure 9 shows the Simulation results of Turbo Encoder.

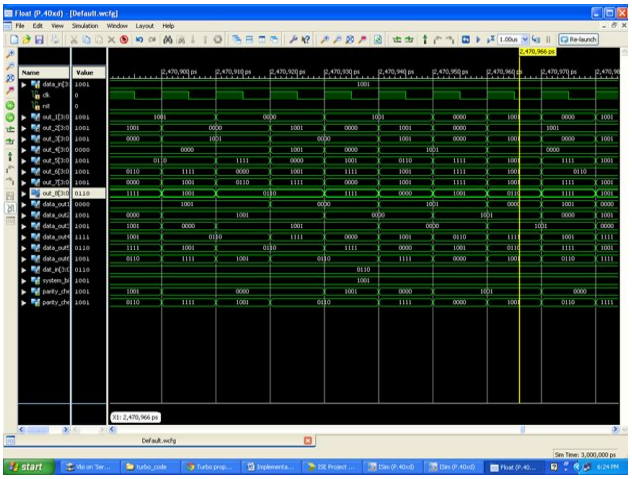

Fig.9. Simulated wave forms of Turbo Encoder

Figure 10 shows the Simulation results of Turbo Decoder.

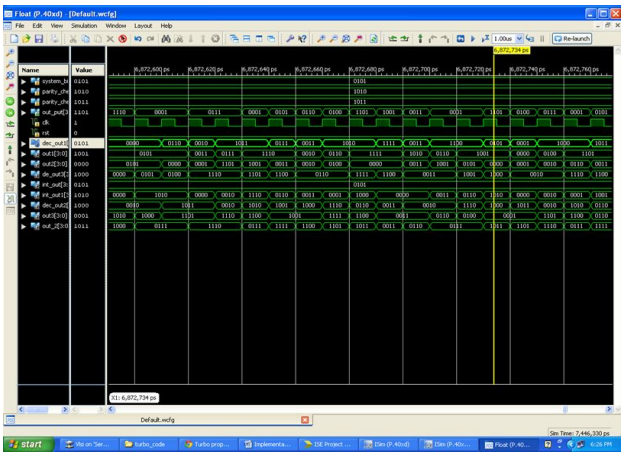

Fig.10. Simulated waveforms of Turbo Decoder

Figure 11 shows the Simulation results of Top Module.

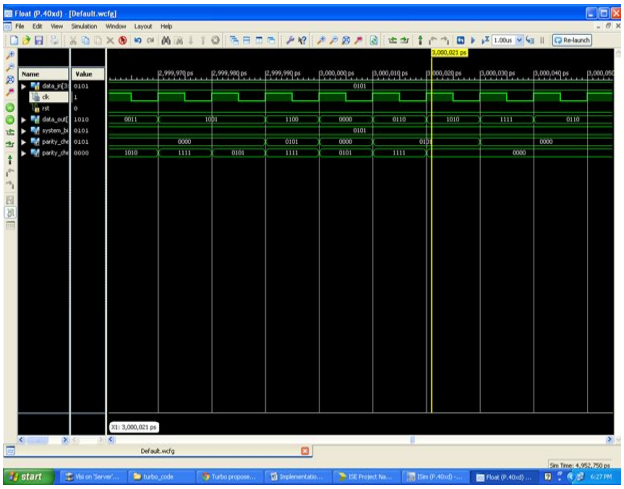

Fig.11. Simulated waveforms of Top Module

Figure 12 shows the power analysis of top module using Cadence encounter (R) RTL compiler.

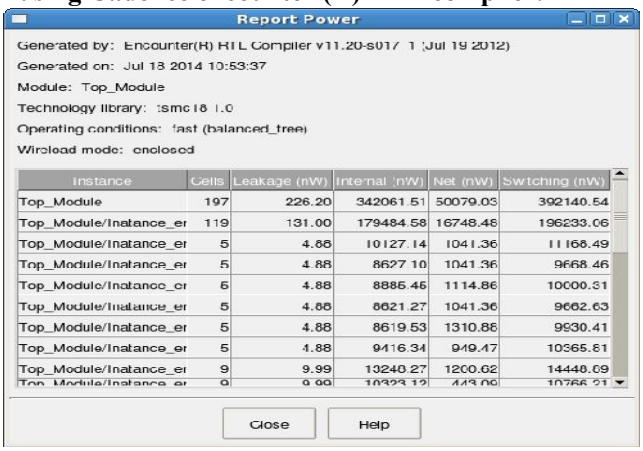

Fig.12. Power analysis of Top Module

Figure 13 shows the Timing Analysis of Top Module using Cadence encounter (R) RTL compiler.

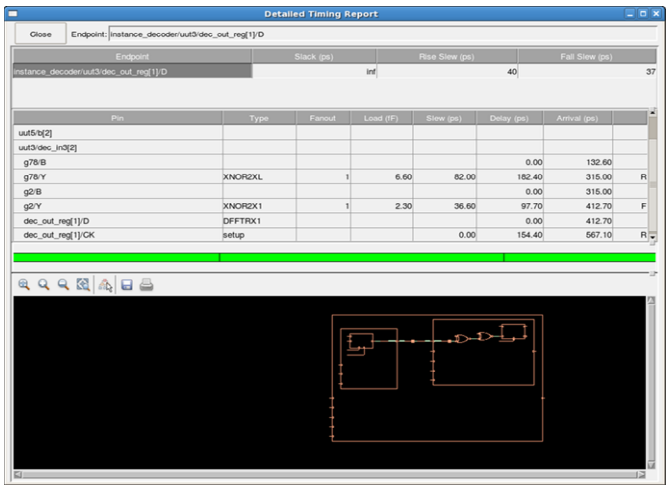

Fig.13. Timing Analysis of Top Module

From the obtained results the proposed architecture consumes a power of 0.0034mW as compared to the existing architecture which consumes power of 4.17mW. Also the proposed architecture is less complex in design.

conclusion

With the excellent performance compared to that of other existing codes, turbo codes and its successors have been adopted into many communication systems and incorporated with various industrial standards. Turbo code applications provide vast coverage of those applications starting from data storage systems through wire-line and wireless communication. That includes the utilization in digital video broadcasting, satellite communications, space exploring systems, and various implementation technologies. Correction of data in different systems for different applications using different techniques is existing in the present system. But we are now using advanced architectures for correction of corrupted or uncorrected data. For the correction we proposed the turbo decoder with the proposed architecture which has been designed, developed and simulated using software tools.

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