A Low Noise Figure and High Gain 6 GHz CMOS LNA with Inductive Source Degeneration Topology

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***Abstract*— This paper presents a 6GHz .18-µm CMOS having low noise figure and good gain LNA which uses an inductive source degeneration topology to have good noise performance, increased gain, and save power consumption. The circuit measurement is performed using UMC .18µm CMOS Technology in cadence tool. The LNA exhibits a noise figure of1.8dB, gain of 18.50dB, S_{11}=--24.dB from1.8V.**

***Index Terms*—** Cascode amplifiers, inductive source degeneration, Noise figure, Input stage cascode circuit.

I. INTRODUCTION

An amplifier is used to increase the strength or power of a signal and depending upon its uses there are various types of amplifiers such as switched mode amplifier, video amplifier etc. And an amplifier used for reducing noise of an electronic circuit is termed as low noise amplifier (LNA). It can also be defined as an electronic amplifier which amplifies very weak signals. By using LNA the effect of noise from the next stage of the receiver is minimized which is typically the first stage of a radio receiver and to provide sufficient gain while introducing least noise possible. Being the first block of the receiver chain LNA has to be able to receive the maximum signal without reflecting any part of it at the same time it has to ensure that it adds less noise to the signal component. The input impedance of the LNA should be 50Ω to match the source impedance, also the output stage should be able to give less noise, and more gain. Since any receiving block's performance depends mainly upon the LNA performance. It is the most important block for any communication system. So a LNA circuit with high gain and very low noise figure is highly needed for any modern receiver system, at the same time it should be less power consuming.

In this paper to have good performance LNA, cascode LNA with inductive source degeneration technique have been proposed. Here CMOS Technology based LNA is used because of its many advantages like CMOS logic reduces power consumption. One of the most important significant of CMOS technology is in RF design which allow to integrate a system on a single silicon chip

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II. LNA topology and Circuit design

One of the widely used LNA in receiver design is the cascade LNA design with inductive source degeneration technique because of its good input matching for both the power gain and the noise figure. Due to its popularity this paper proposed a cascode CMOS LNA employing inductive source degeneration method. Here CMOS technology is used because of its potential for low cost, low static power and the prospect of system level integration.

In any analog circuit design it is mandatory to know some design specification and that specification are standard and our goal is to achieve the desired result. The proposed LNA is designed using a cascade configuration with inductive load.

A. Cascode inductive source degeneration topology

Cascode configuration can be defined as the combination of common source and common gate .To achieve good noise performance and high gain LNA design, widely used technique is cascode inductive source degeneration topology because of its several advantages over other topologies such as good input output matching isolation, better gain, improved bandwidth, good noise performance. And the most important advantage is that it reduces the Miller effect.

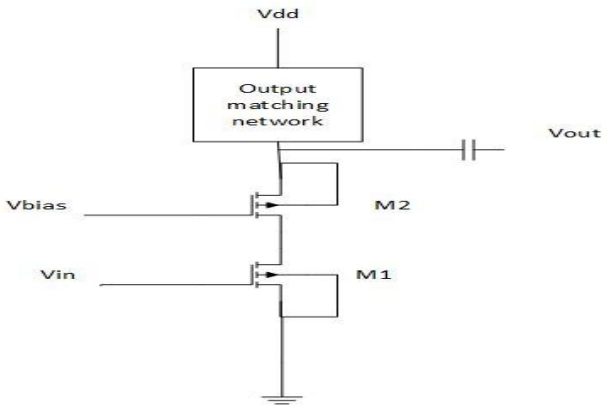

Fig.1. Cascode configuration

In cascode inductive source degeneration instead of using resistive load, an inductive load is used were the inductor connected between the cascode source and the supply blocks any RF leaking. It also acts as bandpass filter which helps in tuning out the capacitance producing at the output. And also it produces less noise compared to the resistive load which is used in other topologies.

B. Input stage cascode circuit

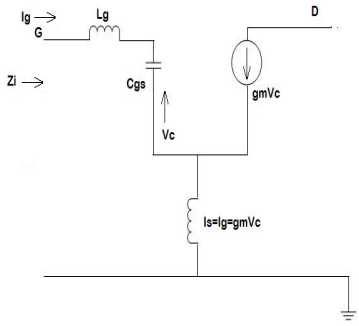

Fig.2. Small signal equivalent of input stage cascode circuit

From the figure, the input impedance Z_i can be calculated as

$$Z_i = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \quad (1)$$

where C_{gs} and g_m are respectively the parasitic gate to source capacitance and the transconductance of M1.

For matching condition,

$$Z_i = Z_s \quad (2)$$

where Z_s is the source impedance whose value is generally made equal to 50 Ω. By solving equation (1) and (2) and equating the real and imaginary part, we get

$$Z_s = \frac{g_m L_s}{C_{gs}} \quad (3)$$

$$s(L_g + L_s) + \frac{1}{sC_{gs}} = 0 \quad (4)$$

Using these equations the value of L_g and L_s is calculated at 6 GHz.

From equation (4) we can obtain input resonance frequency as

$$\omega^2 = \frac{1}{(L_g + L_s)C_{gs}} \quad (5)$$

The most important part of an LNA design is the output impedance stage. As the output of the LNA is feed to the mixer so as to propagate the signal from one block to another block, there should be sufficient impedance matching in between the blocks.

C. Noise figure

Noise figure can be defined as the noise performance of a device at some particular frequency. If a number of components are connected in cascade configuration than the equivalent noise figure of the chain will be

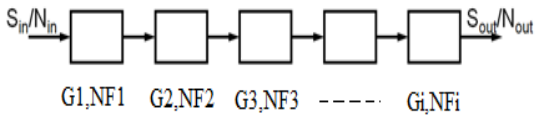

Fig.3. NF of Cascaded Stages

Therefore the total noise figure of the cascaded stage is given by

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \ldots\ldots \frac{NF_i - 1}{G_1 G_2 \ldots G_{i-1}} \quad (6)$$

where NF_1 is the noise figure of the first stage of the cascade stage, G_1 is the gain of the first stage. From the equation above we can say that over noise figure of a cascade stage is dominated by NF_1

Minimum noise can be calculated on the basis of power optimization technique. Applying power optimization technique, the expected noise figure can be obtained by using the formula,

$$F_{min,FD} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_o}{\omega_T}\right) \quad (7)$$

where γ=2 and α=1

Proposed LNA circuit

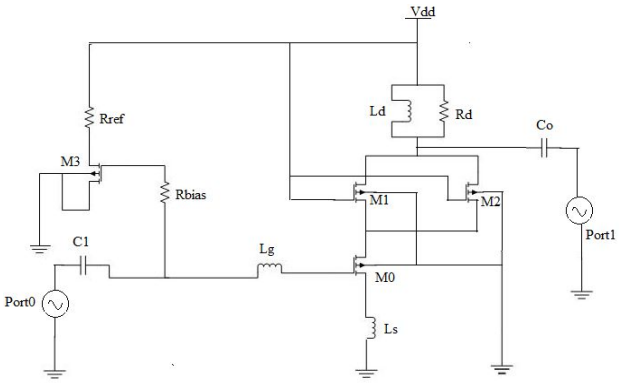

Fig.3 . Proposed LNA circuit

The proposed LNA shown in the figure employed inductive source degeneration in which inductorL_s, is connected to the source of M0. Here L_g,L_s, and $L_d$are all implemented with on-chip spiral inductors $L_g$is gate inductor which is used for tuned out the effect of input capacitance and $L_s$is source degeneration inductor used for input match and $L_d$is drain inductor which provide output resonance with output capacitance and also play an important role in achieving high gain. The inductors $L_g$and $L_s$are chosen in such a way that it provide the desired input resistance This method has the advantage that one has a greater control over the value of the real part of the input impedance through the choice of inductance. Cascoding transistor M0 and M1=M2 is used to reduce the interaction of the tuned output with the tuned input. The RF input is coupled to the gate of the amplifier by the coupling capacitance C0. Transistor M3 is the biasing transistor and forms a current mirror with transistor M0. The width of M3 is

kept a small fraction of the width of M0 to minimize the power overhead of the bias circuit. As shown in fig. we have used R-L tank circuit at the output to increase the stability of the circuit. This tank circuit is used to isolate the amplifier from the capacitive loading effect of the output blocking capacitor. Without Rd the value of Stability Factor (K_f) is less than 1 which exhibits the instability of the circuit. We used ideal components and in ideal components no loss occurs.

III. SIMULATION RESULTS

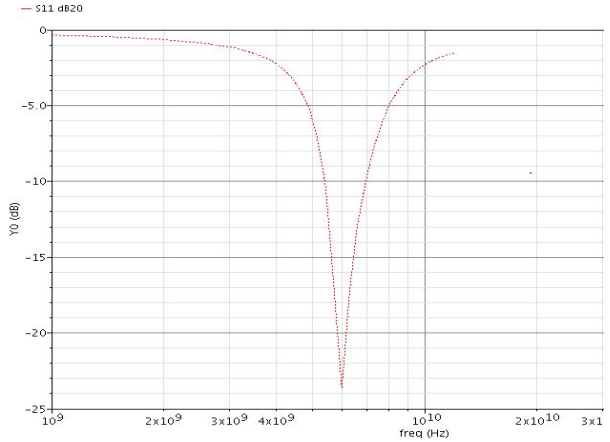

Fig.4. Scattering parameter S11

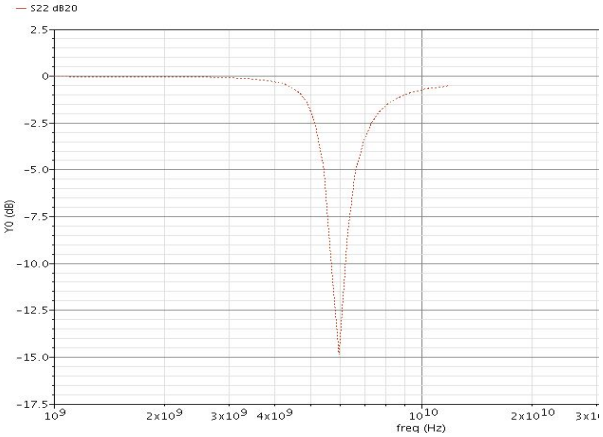

Fig.5. Scattering parameter S_{22}

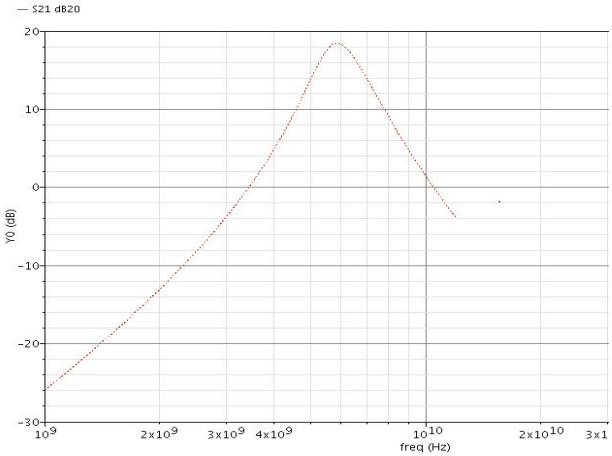

Fig.6. Scattering Parameter S_{21}

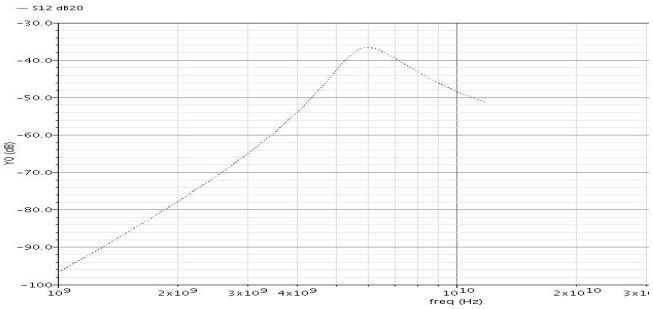

Fig.7. Scattering parameter S_{12}

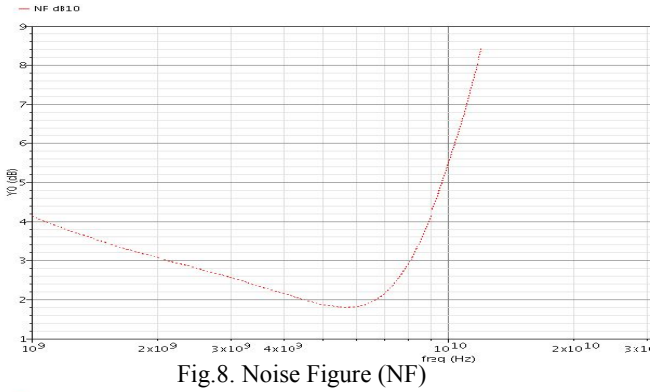

Fig.8. Noise Figure (NF)

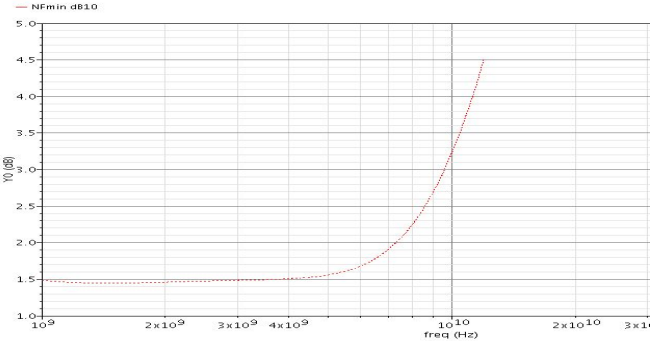

Fig.9. Minimum Noise Figure (NFmin)

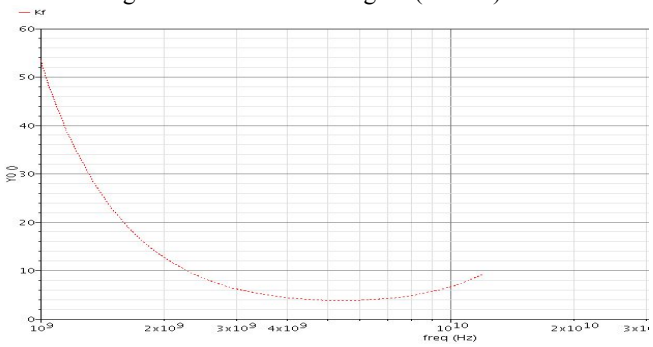

Fig.10. Stability factor

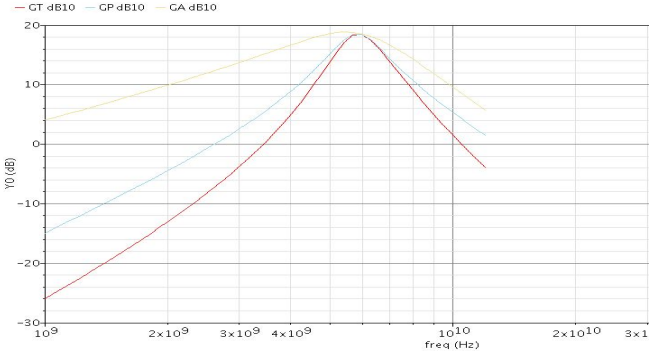

Fig.11. Gain Comparison

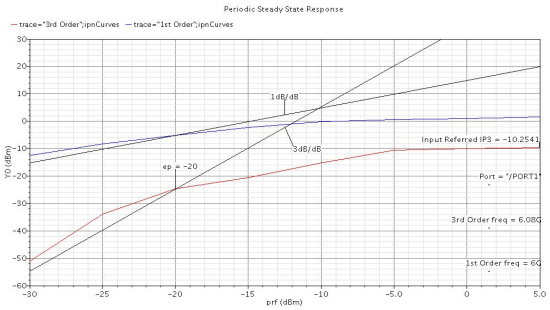

Fig.12.Third order intercept point (IIP3)

IV. DISCUSSION OF THE RESULT

Based on the simulation result Table: 1 shows the various performance parameters result of design

Table: 1 Performance Parameters

Performance parameters	Value	Unit
S_{11}	-24	dB
S_{12}	-36	dB
S_{21}	18.50	dB
S_{22}	-15	dB
Noise Figure(NF)	1.8	dB
Minimum Noise Figure (NF_{MIN})	1.6	dB
Stability Factor(K_f)	4	-
IIP3	-10.2541	dBm

The above table shows the various performance parameters of low noise amplifier, and the value of these parameters after simulation is match and nearly equivalent to theoretically calculated values.

CONCLUSION

In order to design any circuit, it is always better to abstract away its complexity. In this design a low noise amplifier for 6GHz applications covered all the important details required for the general low noise amplifier. And also a novel low noise amplifier is designed and simulated keeping view of high gain and low noise figure for given frequency applications. This design used cascode inductive source degeneration topology as it provided good matching and high gain as compared to other topology. After the simulation we achieved Gain 18.50dB, Noise Figure 1.8dB with very improved linearity and supply voltage is 1.8v.

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Table: 2 Comparison Table

Reference	**This Work**	**[1]**	**[2]**	**[3]**
Gate Length(um)	0.18	0.18	0.35	0.25
Frequency(GHz)	6	5.7	5.2	5.2
S_{11}(dB)	-24	-15	NA	-12
S_{22}(dB)	-15	-9	NA	-12
Gain(dB)	18.50	12.5	19.3	16
Noise Figure (dB)	1.8	3.7	2.4	2.5
IIP3(dBm)	-10.25	-3.3		-1.5
Supply voltage(v)	1.8	1.8	3.3	3

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