Multilevel Inverter Topology with Reduced Number of Switches

D Sai Krishna, M. Harsha Vardhan Reddy

Abstract— Nowadays, multilevel inverters are having wide range of applications. Researchers are also well concentrated on investigating of various topologies for multilevel inverters with less number of switching devices, power supply units and also with fewer harmonic too. In this paper a new multilevel inverter topology is proposed, by which we can generate "6n-5" output levels by using "n" number of capacitors. This proposed topology requires bi-directional switches, one-directional controlled switches, and capacitors. This paper provides a new topology with less number of switches and a single dc source, more number of output levels as compared to conventional multilevel inverters. To validate the proposed topology, MATLAB based simulation analysis and hardware prototypes are carried out.

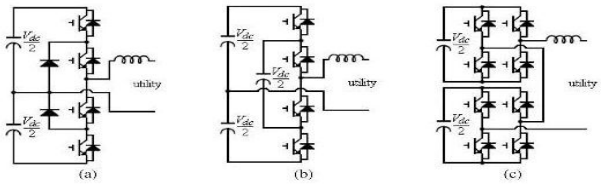
***Index Terms*— Asymmetrical multilevel inverters, Conventional multilevel inverters, Multilevel inverters, Symmetrical multilevel inverters**

I. INTRODUCTION

Nowadays, for high voltage and high power applications, multilevel inverters are preferably used due their advantages like fewer numbers of harmonics, high efficiency etc…. In multilevel inverters, required ac output voltage waveform can be obtained by various combinations of multiple dc voltage sources. As the number of voltage sources increased, the quality of output voltage is much improved.

Multilevel inverters are mainly derived from three basic conventional models [1]. The conventional single phase multilevel inverters include the models of Diode clamped Multilevel inverter or Neutral point Clamped Multilevel inverter, Flying capacitor Multilevel Inverter or Capacitor clamped Multilevel inverter and Cascaded H–Bridge Multilevel Inverter. All three conventional single phase inverters of three level output are shown in Fig(1).

The Neutral point clamped Multilevel inverter has the main drawback of unequal voltage sharing between the series connected capacitors, which leads to dc-link capacitor unbalancing and requires a great number of clamping diodes for a high number of voltage levels [1]. Also, the switching node voltage across the switches will be maximum. The Flying Capacitor multilevel inverter uses capacitors as clamping devices. These topologies have several advantages compared to Neutral point clamped Multilevel Inverters, including the advantage of transformer less operation and have redundant phase leg states that allow the switching stresses to be equally distributed among semiconductor switches [6] and [7].



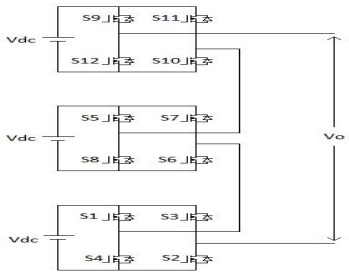
Fig(1). (a) Diode clamped Multilevel inverter (b) Capacitor clamped Multilevel inverter (c) Cascaded H–Bridge Multilevel Inverter

The Cascaded H – Bridge multilevel inverter topologies are a good solution for high-voltage applications due to the modularity and the simplicity of control. But, in these topologies, a large number of separated voltage sources are required to supply each conversion cell. To reduce the number of separate dc voltage sources for high voltage applications, new configurations have also been developed [2-5]. Conventional three multilevel inverters have some particular disadvantages. They need a large number of power semiconductor switches, which increase the cost and control complexity and tend to reduce the overall reliability and efficiency. Although low-voltage rated switches can be utilized in a multilevel inverter, each switch requires a related gate driver and protection circuit. This may cause the overall system to be more expensive and complex. Among these three, cascaded inverters are more advantageous.

Based on the voltage balancing of converter topologies, inverters can also determine as symmetrical inverters [1-3] and asymmetrical inverters [4-5].

In recent years, many configurations are presented in order to reduce the total number of switches and capacitors. Some of them proposed in the literature [2-5]. The main drawback by the use of asymmetrical type of multilevel inverters [4-5] is, here we need an external dc-dc converter to charge the each capacitor, which is used as a small dc power source in inverter circuit. This drawback has been eliminated by series connection of capacitors in this paper.

II. CONVENTIONAL SEVEN – LEVEL INVERTERS



Fig(2). Seven – level Cascaded H–Bridge Multilevel Inverter

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D Sai Krishna, Department of Electrical and Electronics Engineering, GPR College of Engineering (A), Kurnool, India

M. Harsha Vardhan Reddy, Department of Electrical and Electronics Engineering, GPR College of Engineering (A), Kurnool, India

Fig (2), shows the circuit configuration of seven – level cascaded H – Bridge inverter. As can be seen, a seven – level inverter requires 12 IGBT switches and three dc sources. A cascaded H – bridges multilevel inverter is simply a series connection of multiple H – bridge inverters. Each H – bridge inverter has the same configuration as a typical single phase full-bridge inverter.

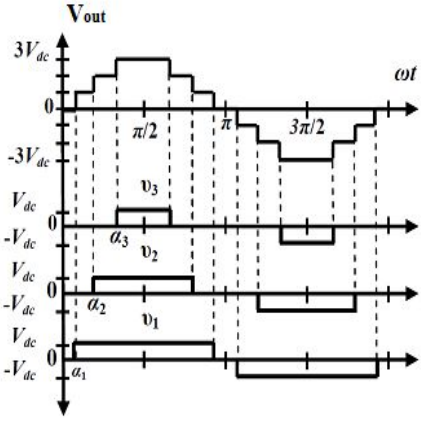
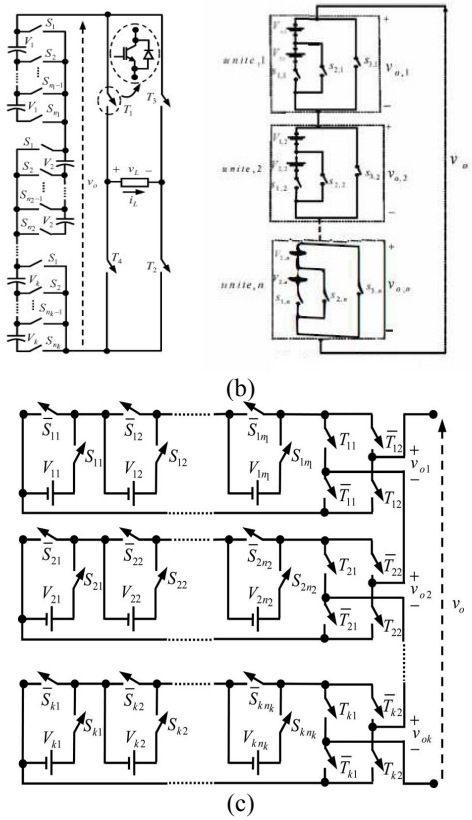


Fig (3). Output Voltage of cascaded H-bridge seven level inverter

The cascaded H-bridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source Vdc. By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced. With this idea, lot of topologies is also developed in recent years. Some of those topologies are presented in literature [2], [4] and [5].



(b)

(c)

Fig. (4). Proposed multilevel converter topology (a) in [2] (b) in [5] (c) in [4]

Fig(4) shows some of recently developed topologies of multilevel inverters. All these topologies are based on developing the positive half – cycles at first and then it fed to an H – Bridge inverter to get an AC output. The proposed topology in this paper is also developed based on this working principle only. The main drawback of all above presented topologies shown in Fig. (4) are they require a separate DC voltage sources for each and every basic unit. If we use only single voltage source, we can replace each voltage source with a significant capacitor, and to charge that capacitor a separate DC to DC converter is required for each capacitor. This drawback can be eliminated in proposed topology presented in this paper.

III. PROPOSED TOPOLOGY

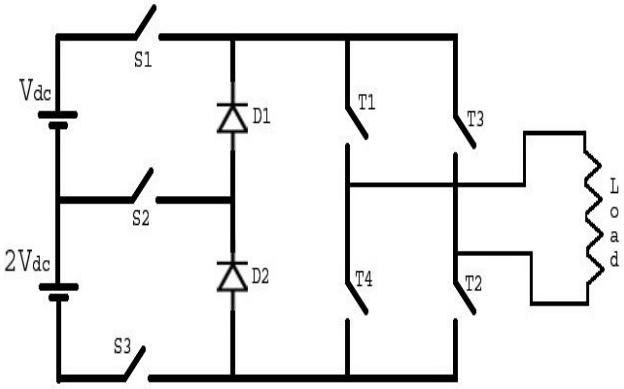
Fig (5) shows the circuit configuration of the seven – level inverter. As can be seen, it is configured with two constant DC voltage sources V1 and V2, seven switches (S1, S2, S3, T1, T2, T3 and T4), where three switches are used at voltage sources for voltage level control and other four used as full bridge inverter for maintaining positive and negative parts of output voltage waveform. Two diodes are also involved in proposed circuit configuration for voltage level controls. Load is connected at the output terminals of full bridge inverter. Proposed circuit other than full bridge inverter generates the output voltage like the output of full wave rectifier as shown in Fig (7). By using fill bridge inverter at the end, all the generated positive half – cycles will be converted into positive and negative half – cycles as shown in Fig (8).

The operation of seven – level inverter can be divided into eight modes. Modes 1 – 4 are for the positive half – cycle, and modes 5 – 8 are for the negative half – cycle. As it can be seen in Fig(5), the power electronic switches in full – bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the DC power into AC power for commutating.

Switches T1 and T2 are turned ON, T3 and T4 are turned OFF during positive half – cycle and switches T3 and T4 are turned ON, T1 and T2 are turned OFF during negative half – cycle. As the constant DC voltage sources are unequal, the magnitude of constant DC voltage sources V1 and V2 can be represented as follows,

V1 = Vdc,

V2 = 2Vdc



Fig(5). Seven – level Proposed Topology

Table (1) is shown all the switching modes and output voltages of seven – level inverter. The modes of operation of proposed seven – level inverter are stated as follows,

Mode1: As shown in Table (1), the output voltage of this mode is 3Vdc (V1+V2). In this mode switches S1 and S3 are turned ON and switch S2 is turned OFF. The diodes D1 and D2 are in reverse bias. Hence in this mode, the load current will have the path through S1 – T1 – Load – T2 – S3.

Mode2: As shown in Table (1), the output voltage of this mode is 2Vdc (V2). In this mode switches S2 and S3 are turned ON and switch S1 is turned OFF. The diode D1 is forward bias and D2 is in reverse bias. Hence in this mode, the load current will have the path through S2 – D1 – T1 – Load – T2 – S3.

Mode3: As shown in Table (1), the output voltage of this mode is Vdc (V1). In this mode switches S1 and S2 are turned ON and switch S3 is turned OFF. The diodes D1 is in reverse bias and D2 is in forward bias. Hence in this mode, the load current will have the path through S1 – T1 – Load – T2 – D2 – S2.

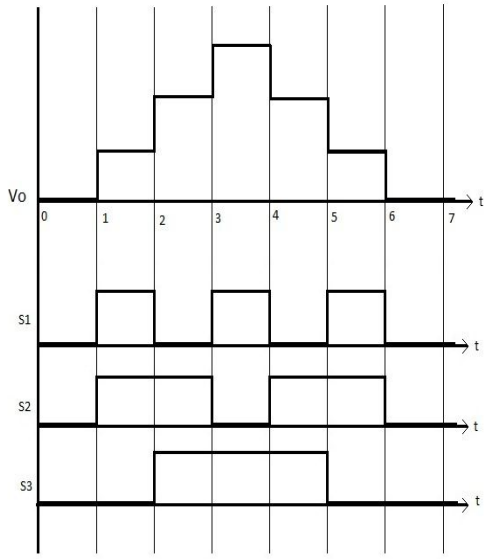
Mode4: As shown in Table (1), the output voltage of this mode is '0'. In this mode switches S1, S2 and S3 are turned OFF. The diodes D1 and D2 are in forward bias. Hence in this mode, the load current will have the path through D1 – T1 – Load – T2 – D2.

Mode	S1	S2	S3	T1T2	T3T4	Vo
1	1	0	1	1	0	3Vdc
2	0	1	1	1	0	2Vdc
3	1	1	0	1	0	Vdc
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	1	1	0	0	1	-Vdc
7	0	1	1	0	1	-2Vdc
8	1	0	1	0	1	-3Vdc

Table (1) Switching Table of Seven – level Inverter

The working principles of mode5, mode6, mode7 and mode8 are similar to mode4, mode3, mode2 and more1 respectively. But as modes 5 – 8 are for negative half – cycle, power electronic switches T1 and T2 turned OFF, T3 and T4 are turned ON in this mode. And the output voltage developed in modes 5 – 8 are 0, -Vdc, -2Vdc and -3Vdc respectively. Hence, the total seven output levels of proposed topology are +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc and -3Vdc respectively.

The switching state waveforms for the positive half cycle of proposed topology are as shown in Fig(6). The positive half cycle of output voltage is divided into seven parts. In each part the output voltage levels are 0, Vdc, 2Vdc, 3Vdc, 2Vdc, Vdc, 0 volts respectively. The total positive half cycle is a period of 0.01sec. with combination of these switches, two more switches in full – bridge inverter are also turned on for the period of 0.01sec, those are T1 and T2. In this period, switches T3 and T4 are in OFF state.

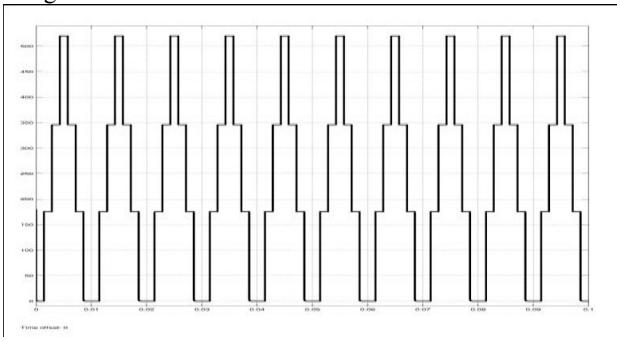


Fig(6). Seven – level Half wave voltage switching waveform

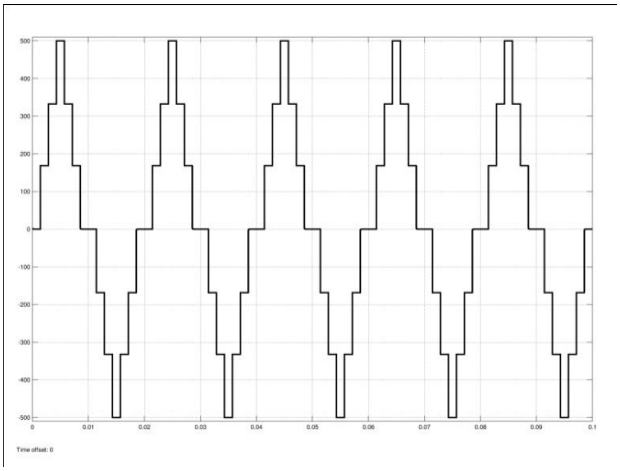
For the negative half cycle of inverter, the above switching patter will be repeated and the switches T3 and T4 are turned on instead of T1 and T2.

IV. SIMULATION RESULT

MATLAB based simulation tool is used to validate the results of proposed topology. 7 – level output voltage is as shown in Figure. Fig(8) shows the final output voltage of 7 – level inverter, and Fig(7) shows the voltage before the full bridge inverter.



Fig(7). Seven – level Half wave output voltage



Fig(8). Seven – level output voltage

All the output voltages are obtained for resistive load of "100Ω". Hence, the current waveforms are also similar to voltage waveforms, but the difference is in magnitude only.

CONCLUSION

In this paper, a new topology has been introduced for cascaded multilevel inverters. The proposed structure is a compound of both bidirectional and unidirectional switches which has the advantage of using fewer IGBTs and deriver circuits. Therefore the proposed topology results in reduction of installation area and cost. The suggested structure extends the design flexibility and possibilities to optimize it for various objectives. The proposed topology has been optimized in this paper for utilizing a minimum number of switches and voltage sources. The results of the simulation for proposed seven – level inverter demonstrate that the proposed configuration has prominent feature compared to other cascaded multilevel inverters.

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Author Information

D. Sai Krishna received B. Tech degree in Electrical and Electronics Engineering from Shri Sai Institute of Engineering and Technology, JNTUA, Anantapur in the year 2012. He is currently pursuing M.Tech in G. Pulla- Reddy Engineering College, Kurnool. His research interests include Electrical Power Converters.

M. Harsha Vardhan Reddy graduated from *Rajeev Gandhi Memorial College of Engineering and technology*, JNTUA, Anantapur in the year 2009. He received M.Tech degree from Karunya Unversity, Coimbatore, India in the year 2011. He is presently Assistant Professor in the Electrical and Electronics Engineering Department, G. Pulla Reddy Engineering College, Kurnool, India. He is currently pursuing Ph.D. in Electrical Engineering Department, JNTU, Hyderabad. His areas of interest include Power Electronics, pulse width modulation Techniques, AC Drives and Control.