Design and Control of Multi Level Inverter with Single DC Source

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***Abstract*— In this project six rules for designing hybrid cascaded multilevel inverters with simplified supply and low switching losses have been derived. These design rules constrain the ratio between the dc voltages of the supplied cells and the dc voltages of the unsupplied cells. They allow one to design single- and three-phase inverters that can be operated either with staircase or with PWM. New configurations that increase the flexibility for choosing suitable switches. The concept of energy balance domain has been introduced to characterize the achievable operating modes and power factor.**

Hybrid asymmetrical cascade multilevel inverters, they combine cells of different voltage ratings different topologies, or even combine switch converters with linear amplifiers. So, in this project mainly focused on the design and control of high-resolution, high-efficiency multilevel inverters with simplified dc power supplies. It introduces several rules for systematically designing the dc voltages of the cells, for which all unsupplied capacitor voltages can be regulated. Six classes of inverters are obtained covering single and three phase, staircase and pulse width-modulated (PWM) inverters.

New configurations of hybrid cascade multilevel inverters are obtained for each class. A double modulation strategy with two different frequencies is proposed that allows switching losses of PWM inverters to be reduced. Decoupled mechanisms are proposed for the total and internal energy balances. It is shown how to make the design robust by taking into account conversion losses and large dc-voltage imbalances in the design and control. The entire proposed system will be tested using MATLAB/SIMULINK.

***Index Terms*— AC-DC power converters, asymmetrical multilevel inverters, cascade multilevel inverters, hybrid multilevel inverters, multilevel converters, multilevel topologies, pulse width modulation converters, series connected converters.**

I. INTRODUCTION

Multilevel inverters have attracted interest for increasing the operating voltage of power conversion devices far beyond the blocking voltage of single switching devices and also for reducing the distortion of the waveforms applied to the load. Among the available topologies cascade multilevel inverters are conceptually the simplest as they combine standard

H-bridge inverters in series. Hybrid asymmetrical cascade multilevel inverters, however, present many challenges as they combine cells of different voltage ratings, different topologies, or even combine switch converters with linear amplifiers.

The main idea behind the hybrid asymmetrical cascade inverter concept is to obtain a better inverter by hybridizing the properties of several cells and switches. In particular, the combination of slow switches, featuring high blocking voltage capabilities and low relative conduction losses, with

fast switches, featuring low switching losses aims at obtaining a hybrid inverter with better equivalent switches that would feature fast switching capability, low conduction losses, and low switching losses. By operating the high-voltage cells at reduced switching frequency, far below the pulse width modulation (PWM) frequency, performing the PWM only with the low-voltage cells, the conversion losses of the inverter alone can indeed be reduced. The main property supporting this result is that the transitions between most pairs of levels involve only the transition of the low-voltage cell. This cannot, however, be achieved for all topologies for all operating points. By designing and controlling the inverter appropriately, it is, however, possible to modulate all pairs of adjacent levels by switching only the low-voltage cells. It has to be noted that the ideas formerly developed for quasi linear amplifiers are conceptually very similar and mathematically yield exactly the same design and control strategies. The concepts for obtaining reduced switching losses have been optimized and generalized for single-phase inverters by the introduction of optimized transition graphs in the switching-state space [9] and for three-phase inverters by introducing the concept of modulation domain.

The supply issues have attracted the attention of many researchers. Rich and Pinero derived design rules for canceling passively the circulation of power between the cells, in order to allow the supply with only rectifiers. Mariethoz and Rufer proposed an efficient multisource dc–dc converter to reduce supply losses. Du et al. investigated how to apply programmed PWM in the context of partially supplied inverter. Lu and Corzine proposed the use of a topology where a motor load serves as isolation between the dc links of two NPC inverters. Steimer and Manjrekar proposed a topology that combines three-phase neutral point clamped (NPC) with unsupplied filtering floating H-bridge cells. Veenstra and Rufer investigated active charging and balancing strategies for this topology based on the control of common mode harmonics. The two main innovations in are the use of a three-phase inverter with a common dc-link as high-voltage cell, and the use of the low-voltage cell only as filtering devices, such that they do not require any additional supply.

This project unifies and completes these works by establishing a theory for systematically designing hybrid cascaded multilevel inverters with simplified dc power supply and low losses. It derives a set of design rules that defines six

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classes of inverters for which an active balance and an efficient modulation can be applied. Inverters with staircase (low frequency) modulation and inverters with PWM (high frequency) are designed in different ways. For the latter, the design rules are extended to take into account losses and voltage imbalances to obtain robust solutions. This project outlines the control of the resulting topologies. The proposed concepts apply for arbitrary reference voltages and currents, not only for sine waves. Finally, the performance of some selected topologies is investigated numerically and experimentally.

II. HYBRID CASCADED MULTILEVEL INVERTER MODEL

A. Investigated Hybrid Cascaded Multilevel Inverter Topologies

This paper investigates the design and control of single- and three-phase hybrid cascaded multilevel inverter topologies for which at least two rows have different voltage ratings and switch technologies and for which only the row with the highest voltage is supplied. Examples of such topologies are represented in Fig.1. For the three-phase topologies,we only consider structures that combine a supplied three-phase cell with unsupplied single-phase cells as for the topologies represented in the following figure.

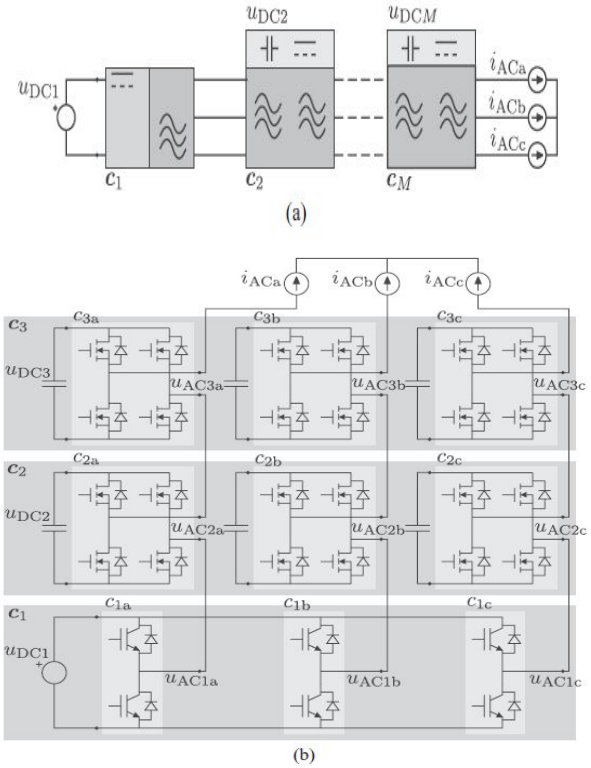


Fig. 1. Investigated three-phase inverter topologies combine one three-phase cell with single-phase cells and thus feature a single dc supply.

(a) General three-phase topology.

(b) Hybrid inverter with two-level three-phase inverter and H-bridges.

The regulation of the voltages of all unsupplied capacitors in these topologies is complex for two main reasons: First, the energy is stored in capacitors that are distributed both over the phases of the inverter and over the cells within a phase. Second, due to the asymmetry of the dc-voltages, the cells of different voltage ratings need to be coordinated to generate the desired output voltage.

For the analysis, the converter is first split between its supplied sub-inverter, which is referred to as the high-voltage cell and its unsupplied sub-inverter, which is referred to as the low-voltage cell. The main difficulty is the energy balance of the low-voltage cell.

B. Necessary Conditions for Energy Balance

There are two necessary conditions for regulating the DC voltages of all unsupplied capacitors to their reference value, while tracking the reference voltage and current trajectories.

1) The total low-voltage cell energy can be regulated only if the low-voltage cell does not provide any active power on average. The high-voltage cell must, therefore, provide the total power on average, while the low-voltage cell can only provide reactive, harmonic, and transient powers.

2) The dc-voltages can be regulated only if the distribution of energy within the low-voltage cell over its phases and rows can be modified, while preserving the inverter target output voltage.

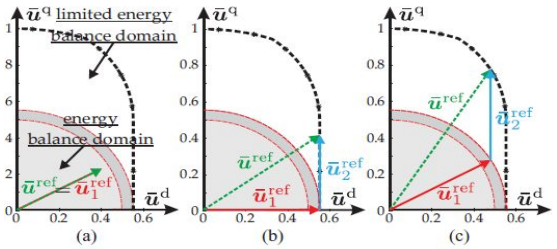


Fig.2.Voltage breakdown on average in the dq plane oriented on load current. Mode of operation depends on reference magnitude.

These conditions limit the operating range of the converter, and require special design and control procedures that will be developed in Sections III–VI.

C. Operating Modes

The first necessary condition for balancing the total low voltage cell energy requires the high- and low-voltage cells to operate in one of the modes below.

1) For space-vector references smaller than the high-voltage cell maximum magnitude, the high-voltage cell is able to provide the full-voltage on average; the low-voltage cellonly needs to provide harmonic filtering that allows it toprecisely generate the reference [see Fig. 2(a)].

2) For space-vector references exceeding the high-voltage cell maximum magnitude, the maximum power factor can be reached by keeping the high-voltage cell contribution parallel to the current, while the low-voltage cell provides a voltage contribution orthogonal to the space-vector current on average, in order to increase the inverter achievable voltage magnitude [see Fig. 2(b)].

3) The maximum magnitude can be reached by contributing to the orthogonal component of the voltage with both high voltage and low-voltage cells:

the achievable power factor is lowest in this mode [see Fig. 2(c)].

The analysis of these operating modes leads to two definitions that will be useful through our developments.

1) Energy balance domain: This is the set of voltage vectors,represented in light gray in Fig. 2, that can be reached by the high-voltage cell alone on average. There is no or little restriction on the current waveform for trajectories fully belonging to this set. If the converter were only operated in this region, the capacitor could be very small, ideally close to zero. For steadystate operation, a larger set can be defined that corresponds to the set of voltages for which any power factor can be achieved, that is represented in Fig. 2 by augmenting the previous set with the dark gray area.

2) Limited energy balance domain: This is the set of voltages vectors that can be reached by the converter but that are not in the energy balance domain, represented by the area below the black bold dash curve in Fig.2. The current trajectory for these vectors must be cyclic and fulfills some restrictions. In steady-state operation, this corresponds to a restriction on the

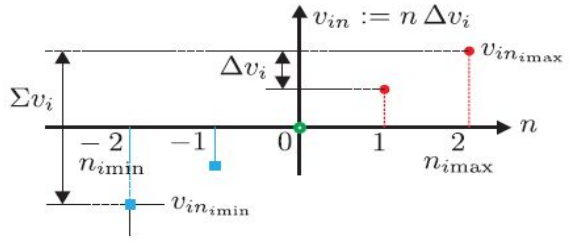


Fig.3. Key parameters defining the properties of a multilevel cell.

achievable power factor and magnitude. In this domain, the ability to exchange power between phases is very limited. The capacitors,therefore, need to be sufficiently large to ensure that the voltage ripple remains small while storing the energy required for providing reactive and harmonic power over each cycle. It should be noted that since the generation of reactive currents does not need any active power (on average), the capability of the inverter will always be higher in the q-axis as suggested in Fig.2. The maximum achievable magnitude, i.e., the size and shape of the limited energy balance domain depends on the topology and the selected configuration (see Section VII-B for further details on this aspect).

III. DESIGN CONDITIONS FOR ENERGY BALANCE

To balance the low-voltage cell total energy, it is sufficient to operate the converter in one of the three modes described previously in Section II-C. To achieve this, while ensuring that the target space vector is generated at the output of the converter, it is necessary to follow the design rules that will be derived in this section. The keys underlying total and internal balance, while guaranteeing the tracking of the reference level trajectory, independently of the current trajectory, are the design and exploitation of redundant space vectors to adjust the cell power flows.To simplify the explanations, we will consider two series-connected cells, without loss of generality, since we can repeat the reasoning by associating two series-connected cells in a larger cell that would become the new low-voltage cell in the reasoning. In addition, we will exploit the latter property to derive the results presented in Section VIII. We will first derive the design rules for single-phase inverters and then for three-phase inverters.

A. Single-Phase Energy Balance Design Condition

c_{ij} N_i Δv_i $\Delta v_i = u_{DCi}$ n c_{ij} $v_{in} = n\Delta v_i$ n $[n_{imin}, n_{imax}]$ i $i \in \{1, \ldots, M\}$ M j $j \in \{a, b, c\}$ v_{in} j i u_{ACij} s_{ij} $u_{ACij} = v_{in}$ $s_{ij} = n$

,Δv1), . . . , (NM ,ΔvM)}. The topology

$$u_{ACj} = \underbrace{\sum_{i=1}^{M} u_{DCi}\, s_{ij}}_{\text{level realization } v_o} + \underbrace{\sum_{i=1}^{M} \epsilon_{DCij}\, s_{ij}}_{\text{error } \epsilon}. \qquad (1)$$

v_o v_o *rigorously exist*

v_{1k} v_{1m} v_{2l} v_{2n} v_o

$$\underbrace{v_{1k} + v_{2l}}_{\text{first realization of } v_o} = \underbrace{v_{1m} + v_{2n}}_{\text{second realization of } v_o} = v_o. \qquad (2a)$$

k m $[n_{1min}, n_{1max}]$ l n $[n_{2min}, n_{2max}]$ v_o λ

v_o .u_{AC2}

v_{2l} v_{2n}

$$v_{2l} \leq \underbrace{\lambda v_{2l} + (1-\lambda) v_{2n}}_{\text{average contribution } \bar{u}_{AC2}} \leq v_{2n}. \quad (2b)$$

v_{2l} i_{ACj}

v_{2n} i_{ACj} λ

v_{2l} v_{2n}

v_{2l} v_{2n}

λ

v_{2l}

v_{2n} i_{ACj}

v_{2n} i_{ACj}

v_{2l} v_{2n}

v_{1k}

v_{1k+1}

$$\Delta v_1 \leq \frac{N_2+1}{2} \Delta v_2. \quad (3)$$

$[v_{1n1m\,in}, v_{1n1m\,ax}]$

B. Three-Phase Energy Balance Design Condition

i

c_{ia} c_{ib} c_{ic} c_i

c_i

$$u_{ACi} = u_{DCi} s_i + \epsilon_i \quad (4a)$$

$$s_i = T_{abc}^{\alpha\beta} \begin{bmatrix} s_{ia} & s_{ib} & s_{ic} \end{bmatrix}^T \quad (4b)$$

v_o

$$\epsilon_i = T_{abc}^{\alpha\beta} \begin{bmatrix} s_{ia}\epsilon_{DCa} & s_{ib}\epsilon_{DCb} & s_{ic}\epsilon_{DCc} \end{bmatrix}^T \quad (4c)$$

$T_{abc}^{\alpha\beta}$

c_i

$$p_{ACi} = u_{ACi}^T i_{AC}. \quad (4d)$$

c_{ij}

c_i

$T_{abc}^{\alpha\beta}$

IV. DESIGN CONDITIONS FOR ENERGY BALANCE AND LOW SWITCHING LOSSES

In the previous section, design rules that guarantee sufficient redundant realizations for each level and space vectors to regulate the voltages of the low-voltage cells were derived. The modulation of redundant vectors was used to balance the cells.PWM operation of different voltage vectors to smoothly control the output voltage can readily be superimposed using the same balancing concepts, but it may result in excessive switching losses due to the operation of the high-voltage cells at the PWM frequency. Design conditions to operate the high-voltage cells at low switching frequency have already been derived for single-[9] and for three-phase inverters [10], but without considering energy balance. This section derives design rules that allow the low-voltage cell energy balance and the optimal operation of the high-voltage cell at low switching frequency.

A. DOUBLE MODULATION PRINCIPLE

The balance principle elaborated in the previous section modulates redundant realizations of the target space vector vo with the duty cycles λr to control the low-voltage cell stored energy by manipulating the output voltage breakdown over the cells. It is worth stressing the difference between this balance modulation and the synthesis of a reference space vector voltage uref AC using PWM. The first does not affect the output voltage, while the latter requires the modulation of several space vectors with the duty cycles d. To synthesize a reference space-vector voltage uref AC using PWM, while regulating the unsupplied capacitor voltages, two modulations with two different objectives need to be combined. The modulation that regulates the dc voltages does not need to be very fast, since it deals with the balance of relatively large capacitors with long time constants, while the synthesis of the target space vector needs to be very fast since it usually deals with fast dynamics. By design, the balancing modulation requires that the high-voltage cell switches when the inverter switches from one realization of a space vector to another. In the ideal case, it would be necessary to switch the high-voltage cell space vector only at low frequency, either for the balance or when changing the set of modulated space vectors, but not during the output space-vector synthesis that would require operation at the PWM frequency. The corresponding double modulation principle is represented in Fig. 4. We will

investigate how to design the inverter to be able to apply this double modulation with two different switching frequencies in Sections IV-B and IV-C.

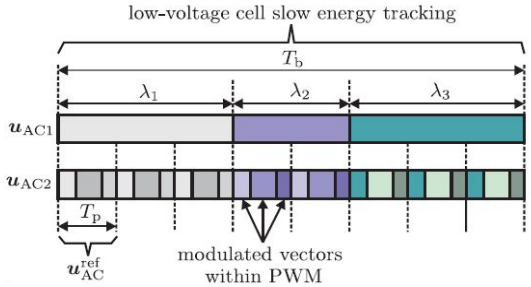


Fig. 4. Double modulation principle: the duty cycles λ1,2,3 that allow one to regulate the capacitor voltages and the duty cycles d1,2,3 that allow one to synthesize the reference are operating at two different frequencies in order to minimize the hybrid inverter switching losses.

B. Single-Phase Energy Balance and Low-Switching Loss Design Condition

*u*ref

*v*o *v*o +Δ *v*2

d

$$u_{AC}^{ref} = v_o + d\,\Delta v_2. \quad (5)$$

*v*2*l* *v*2*l* +Δ *v*2

$$u_{AC}^{ref} = v_{1k} + v_{2l} + d\ \Delta v_2$$

*v*2*l* *v*2*l* +Δ *v*2

$$u_{AC}^{ref} = v_{1m} + v_{2n} + d\,\Delta v_2, \quad v_{1m} = v_{1k} + \Delta v_1$$

*v*2*n* *v*2*n* +Δ *v*2

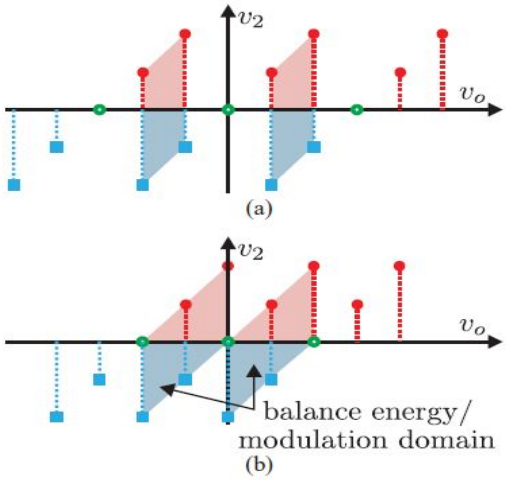
d

λ

$$\bar{u}_{AC1} = \lambda v_{1k} + (1-\lambda) v_{1m}$$
$$\bar{u}_{AC2} = \lambda v_{2l} + (1-\lambda) v_{2n} + d\,\Delta v_2$$

) with the duty cycle λ, the

$$\Delta v_1 \le \frac{N_2 - 1}{2} \Delta v_2$$



C. Three-Phase Energy Balance and Low-Switching Loss Design Condition

$$\Delta v_1 \le (N_2 - 1)\Delta v_2$$

$$\Delta v_{i+1} \le \sum_i (N_i - 1)\Delta v_i$$

V. THREE-PHASE LOW-VOLTAGE CELL INTERNAL BALANCE OVER PHASES

total energy

$$[u_{ACia}^{\perp} \quad u_{ACib}^{\perp} \quad u_{ACic}^{\perp}][i_{ACa} \quad i_{ACb} \quad i_{ACc}]^T = 0$$

u AC*i*0

$\alpha\beta$

$\alpha\beta$

$$u_{\mathrm{ACi}}^{\perp\ T} i_{\mathrm{AC}} = [u_{\mathrm{ACi}\alpha}^{\perp} \quad u_{\mathrm{ACi}\beta}^{\perp}][i_{\mathrm{AC}\alpha} \quad i_{\mathrm{AC}\beta}]^T = 0$$

A. Compensation Through Common-Mode Voltage

$$\Delta p_{\mathrm{a}} = u_{\mathrm{AC}i0}\, i_{\mathrm{ACa}}$$
$$\Delta p_{\mathrm{b}} = u_{\mathrm{AC}i0}\, i_{\mathrm{ACb}}$$
$$\Delta p_{\mathrm{c}} = u_{\mathrm{AC}i0}(-i_{\mathrm{ACa}} - i_{\mathrm{ACb}})$$

$u_{\mathrm{AC}i0}$

$u_{\mathrm{AC}i0}$

$$\min_{u_{\mathrm{AC}i0}(t)} \sum_{j\in\mathrm{a,b,c}} e_{ij}(t+T_{\mathrm{h}})^2$$

e_{ij} c_{ij} t

$$e_{ij}(t+T_{\mathrm{h}}) = e_{ij}(t) + \left(u_{ij}^{\mathrm{ref}}(t) + u_{\mathrm{AC}i0}(t)\right) i_{\mathrm{AC}j}(t) T_{\mathrm{h}}$$

T_{h}

B. Compensation in the αβ Plane

$\alpha\beta$

$\alpha\beta$

VI. EXPERIMENTAL RESULTS

1) Hardware Prototype:

2) Software prototype:

B. Five-Level Hybrid Cascaded Multilevel Inverter Drive Results

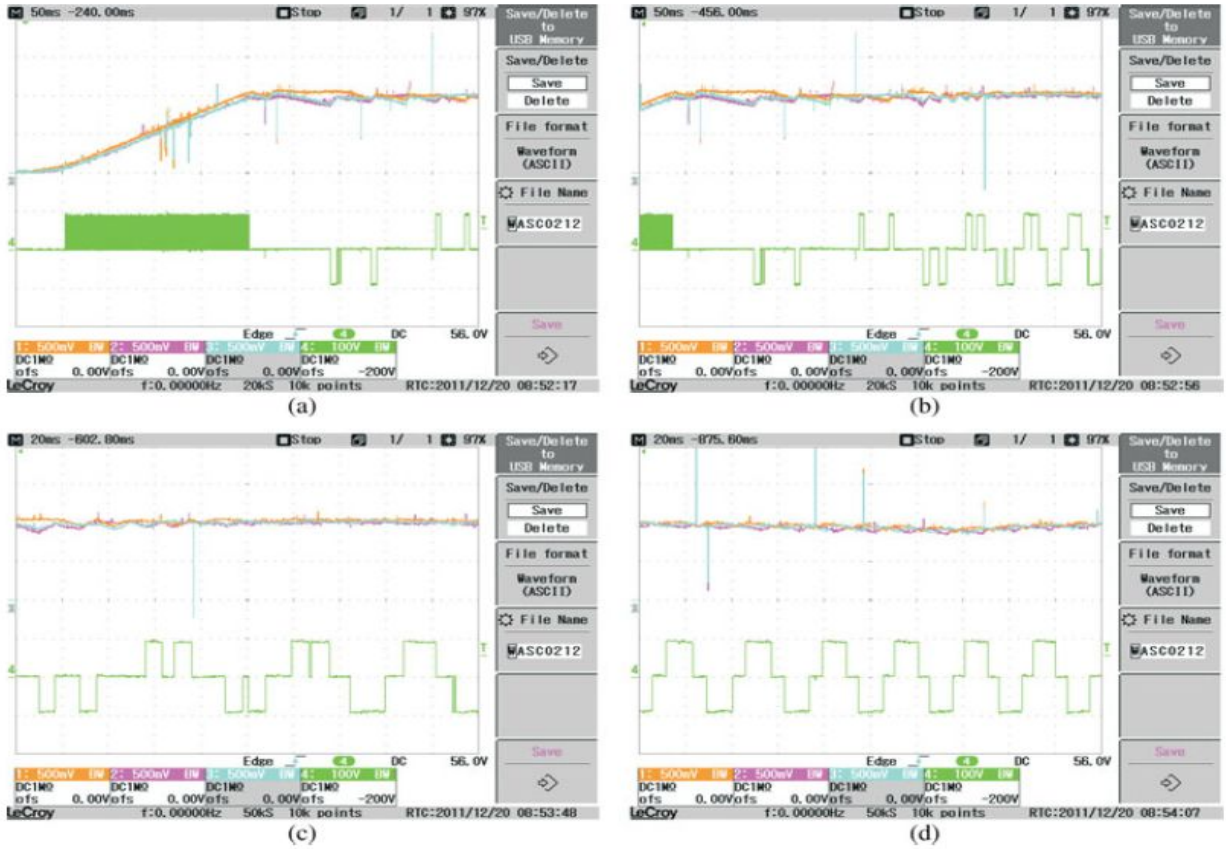
c 3

u_{DC2} =

u_{DC1} = 90

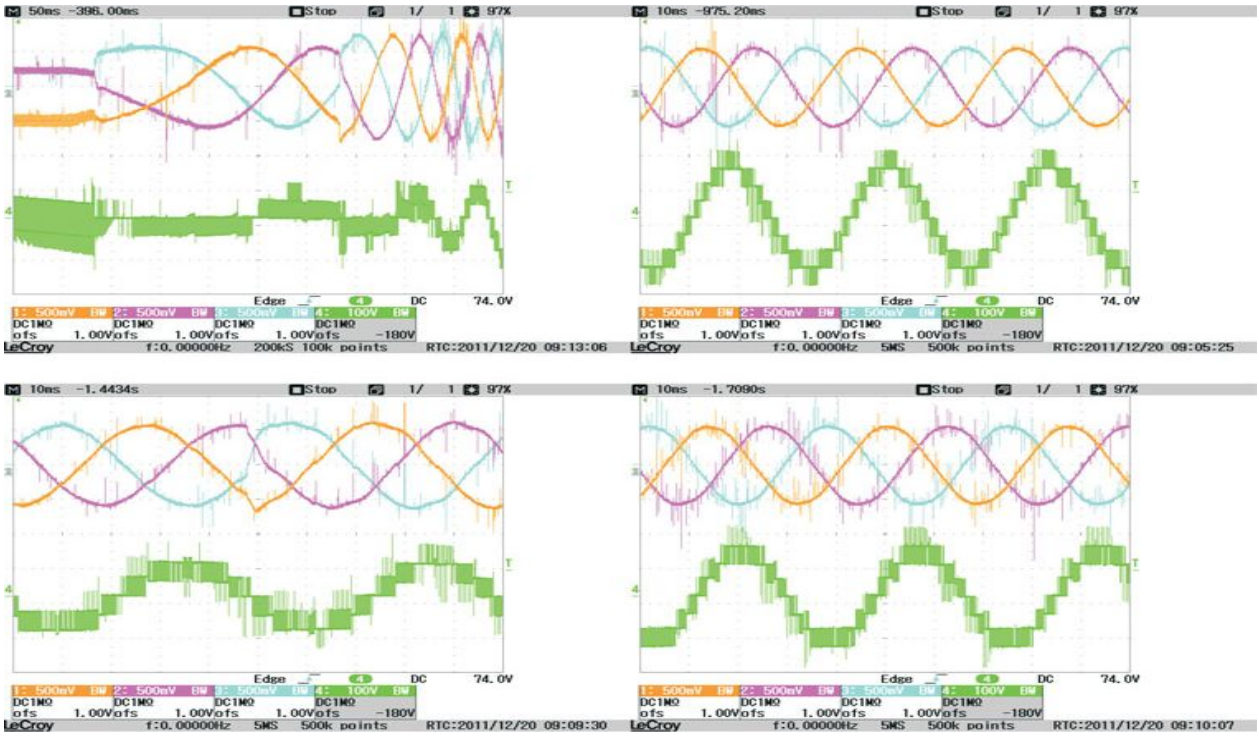
1) Voltage Regulation During Precharge:

2) Voltage Regulation During Normal Operation:



1 3

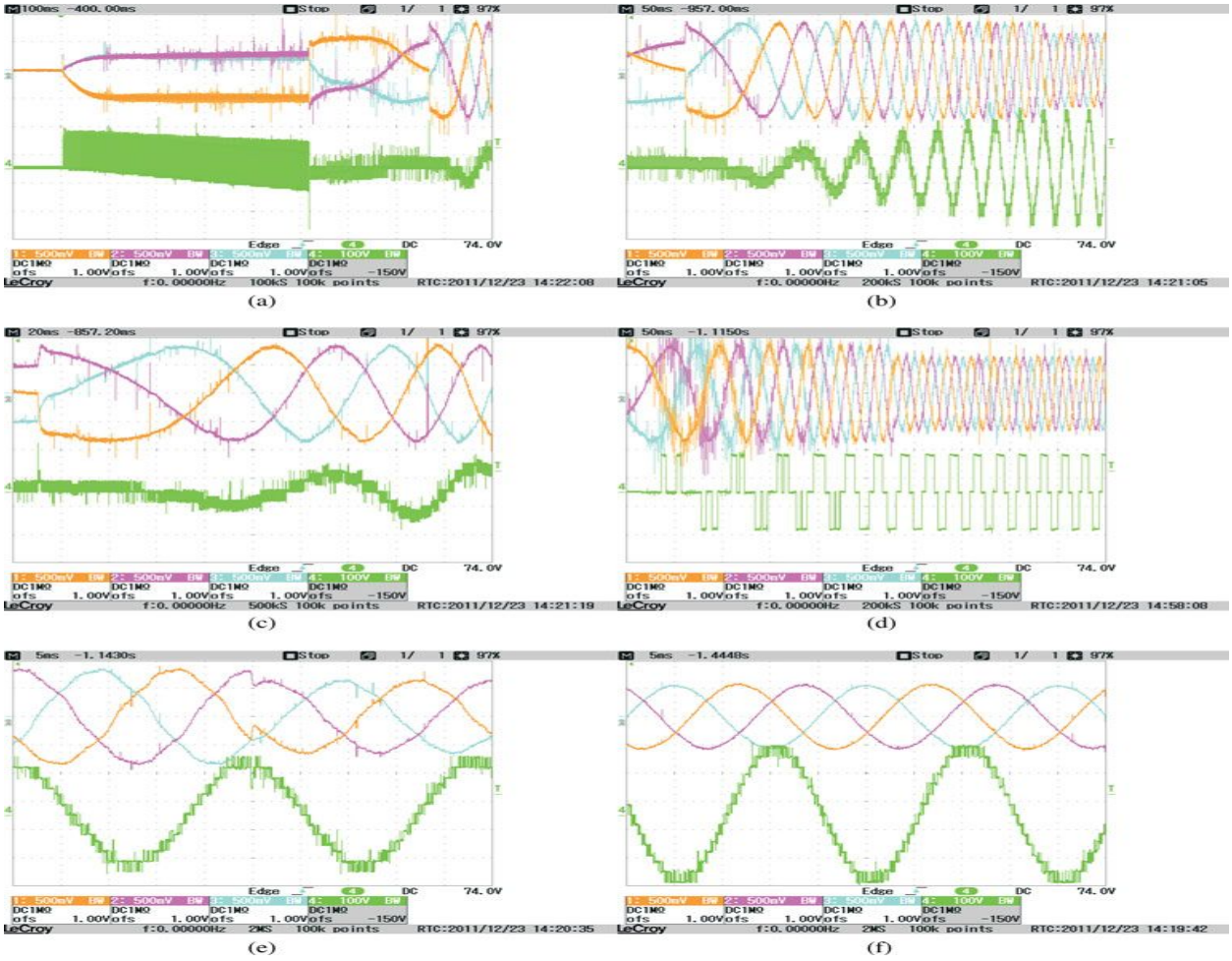
4



1 3 4

$t \in [100, 320]$

t = 800 I_{qref} t = 1000 I_{qref} –



1 3 4

i_{qref} = 2.8 i_{qref} = 1.2

:

6) Voltage Balance:

:

CONCLUSION

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