International Journal of Engineering Research And Management (IJERM)
ISSN : 2349- 2058, Volume-02, Issue-02, February 2015

Efficiency of DC-DC Buck Boost Converter with Mode Select Circuit and Soft Switching Techniques

K.Kishore, Dr.M.Sridhar

***Abstract*— This paper presents a high efficiency positive buck–boost converter with mode-select circuits and feed-forward techniques. Four power transistors produce more conduction and more switching losses when the positive buck–boost converter operates in buck–boost mode. Utilizing the mode-select circuit, the proposed converter can decrease the loss of switches and let the positive buck–boost converter operate in buck, buck–boost or boost mode. By adding feed-forward techniques, the proposed converter can improve transient response when the supply voltages are changed. The proposed converter has been fabricated with TSMC 0.35µm CMOS 2P4M processes. The total chip area is 2.59 × 2.74 mm2 (with PADs), the output voltage is 3.3 V, and the regulated supply voltage range is from 2.5–5 V. Its switching frequency is 500 kHz and the maximum power efficiency is 91.6% as the load current equals 150 mA.**

***Index Terms*— Feed-forward techniques, mode select, positive buck–boost converter.**

I. INTRODUCTION

The development of semiconductor manufacturing technology, conversion efficiency, power consumption, and the size of devices have become the most important design criteria of switching power converters [1]–[9]. Power converters are often applied to LED products, notebooks, mobile phones, and car electronics products. For portable applications, in order to provide consumers better conveniences, how to extend battery life and improve the conversion efficiency of power converters are challenges for designers. Therefore, it is essential to develop accurate switching power converters, which can reduce more wasted power energy [10].The positive buck–boost converter can operate in buck mode,
buck–boost mode, and boost mode.
we design a mode-select circuit to detect the battery energy $V_{battery}$ and select the operation mode. When the converter operates in buck mode or boost mode, it only switches two power transistors. The mode-select circuit can reduce the conduction loss and switching loss of the proposed converter, and the power efficiency can be improved [11]–[17].

Manuscript received February 15, 2015.

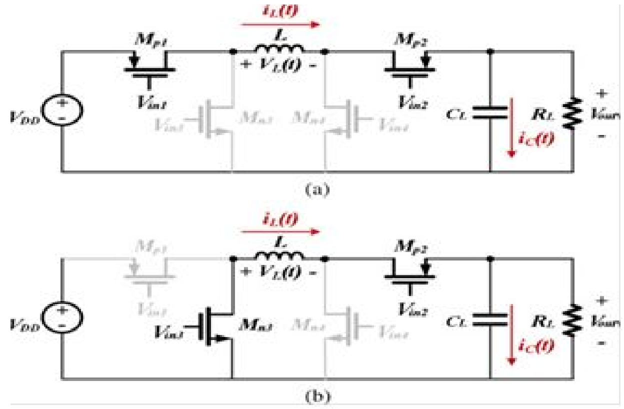


Fig. 1. (a) Charging interval.
(b) Discharging interval of buck mode.

The proposed converter can operate in wide supply voltage range and extend the battery life. Fig. 1(a) shows the proposed converter operating in the charging interval of buck mode; the power transistors Mp1 and Mp2 are turned ON and the power transistors Mn3 and Mn4 are turned OFF. Fig. 1(b) shows the proposed converter operating in the discharging interval of buck mode; the power transistors Mp2 and Mn3 are turned ON and the power transistors Mp1 and Mn4 are turned OFF. Fig. 2(a) shows the proposed converter operating in the charging interval of buck–boost mode; the power transistors Mp1 and Mn4 are turned ON and the
power transistors Mp2 andMn3 are turned OFF.
Fig. 2(b) shows the proposed converter operating in the discharging interval of buck–boost mode;the

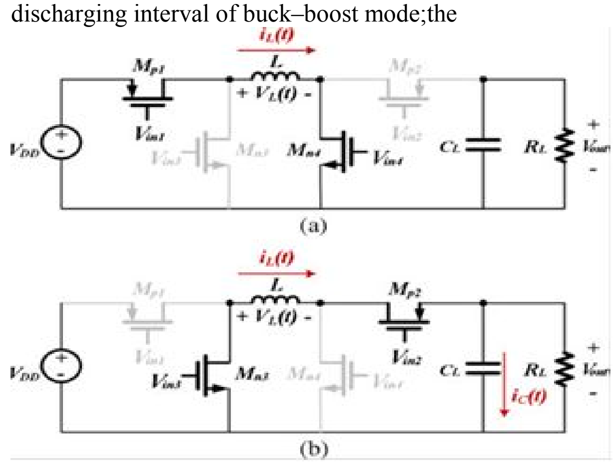
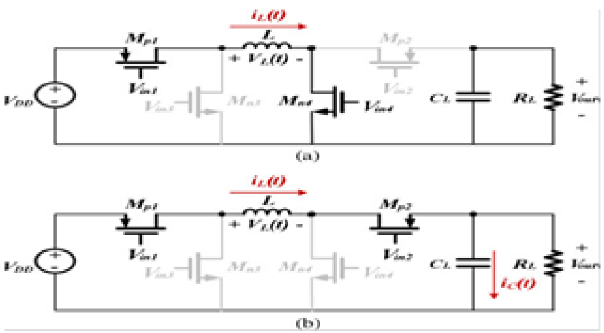


Fig.2. (a) Charging interval.
(b) Discharging interval of buck–boost mode.

power transistors Mp2 and Mn3 are turned on and the power transistorsMp1 andMn4 are turned off. Fig.3(a) shows the proposed converter operating in the charging interval of boost mode; the power transistors Mp1 and Mn4 are turned ON and the power transistors Mp2 and Mn3 are turned OFF.

Fig. 3(b) shows the proposed converter operating in the discharging interval of boost mode; the power transistors Mp1 andMp2 are turned ON and the power transistorsMn3 andMn4 are turned OFF. In this paper, the circuit description of the proposed is
shown in Section II, and the experimental results are shown in Section III. Finally, the conclusion is made in Section IV.

II. CIRCUIT EXPLINATION



V_b

V_{DD} V_c V_{add}

V_{DD}

V_p

V_{buck} V_{boost}

A. Analog-Adder Circuit

V_{DD}

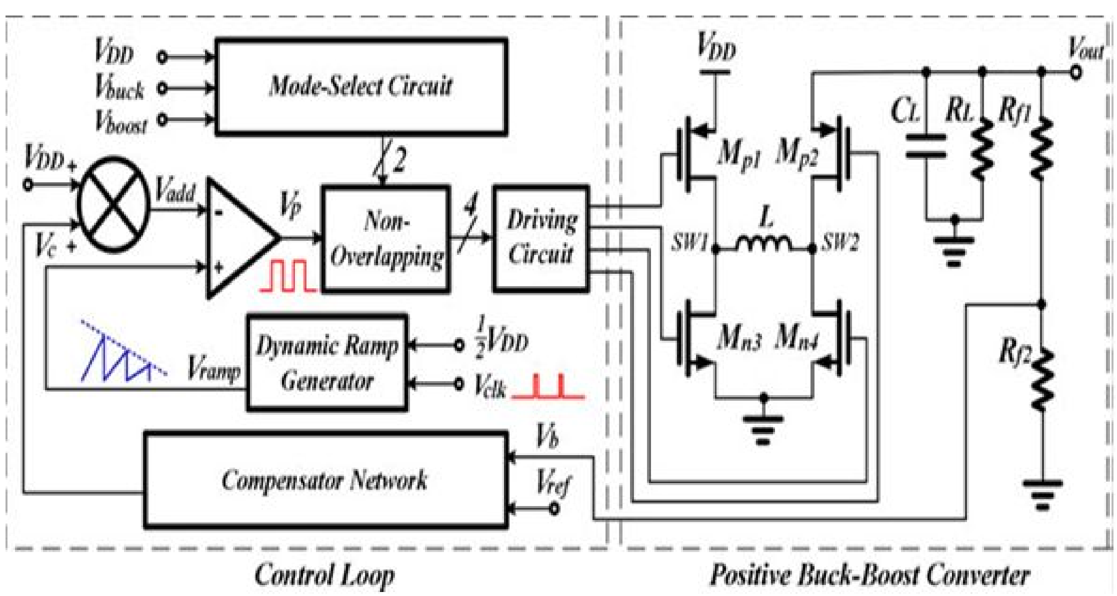
V_c V_{add}

V_c

V_{DD}

$$V_{add} = \left(1 + \frac{R_b}{R_a}\right)\left[\frac{(R_d//R_e)}{R_c + (R_d//R_e)}V_c + \frac{(R_c//R_e)}{R_d + (R_c//R_e)}V_{DD}\right].$$

B. Mode-Select Circuit



C. Dynamic Ramp Generator

V_{clk}

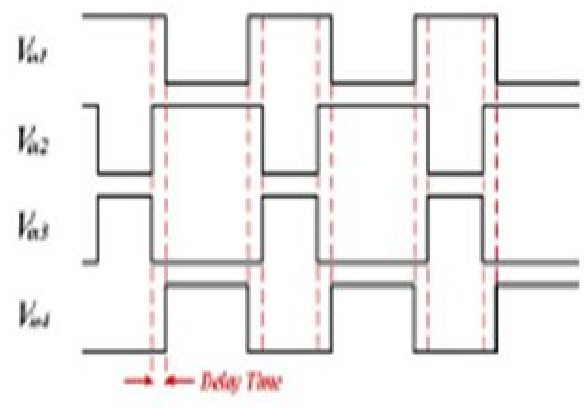
V_{clk} M_{n6} C_t V_{clk}
M_{n6} C_t

D. Compensator Network

$$\frac{V_c}{V_{out}} = \frac{(1+sC_{c2}R_{c2})(1+sC_{c1}R_{c1})}{(sC_{c2})\left[(R_{f1}//R_{f2})+R_{c1}\right]\left[1+s\frac{C_{c1}R_{c1}(R_{f1}//R_{f2})}{(R_{f1}//R_{f2})+R_{c1}}\right]}$$

V_{out} V_{ref}
V_c

E. Non overlapping Circuit



F. Level Shifter Circuit

V_{out} V_{DD}
M_{p2} V_{out}
V_{DD}
M_{p2}

V_{DD}
V_{out}
V_{DD}
V_{DD} V_{out}

V_{out}

G. Driving Circuit

III. EXPERIMENTAL RESULTS

μ

$\times$

V_{DD}

V_{out}

V_{DD}

V_{out}

V_{DD}

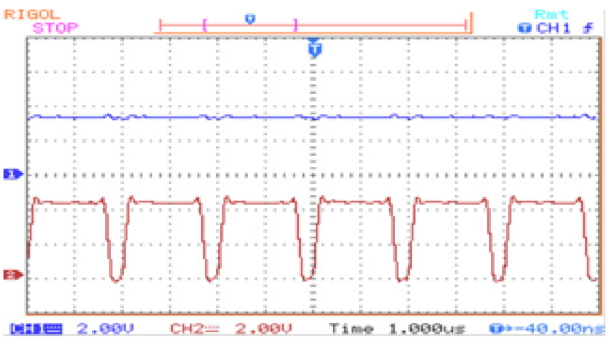
V_{out}

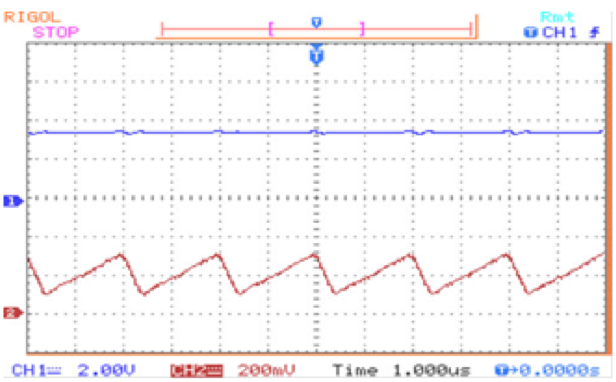
V_{DD}

V_{out}

V_{DD}

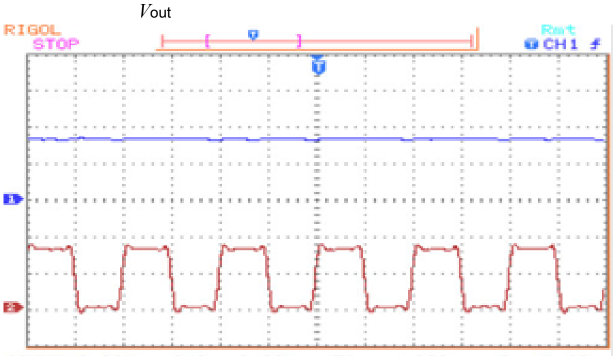
V_{out}





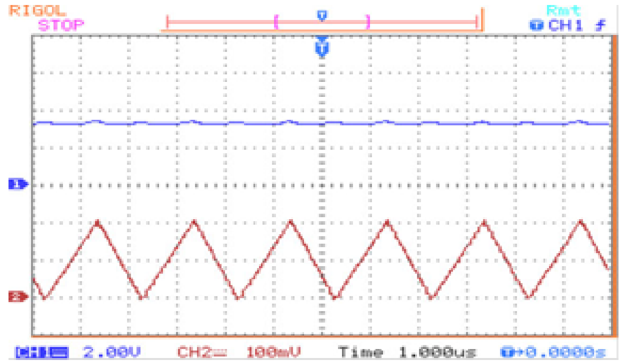
V_{DD}

V_{out}



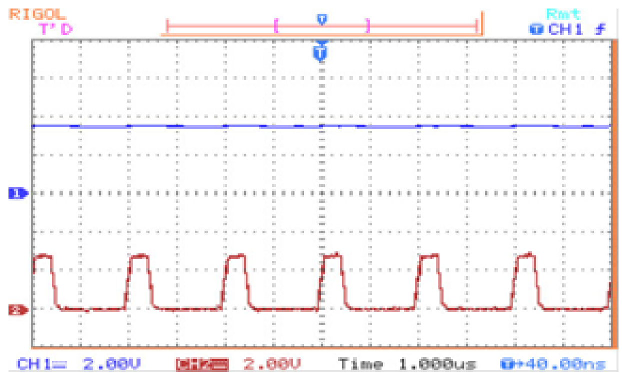
V_{DD}

V_{out}



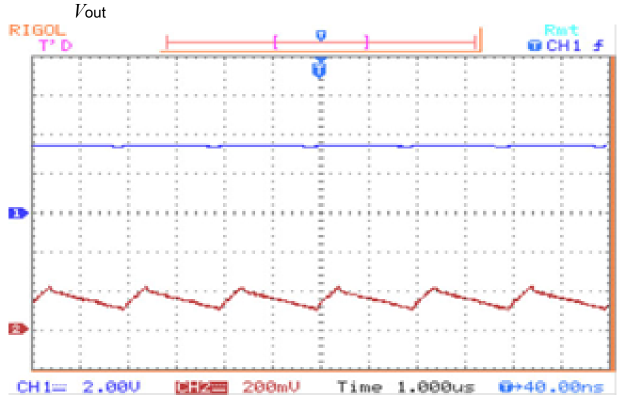
V_{DD}

V_{out}



V_{DD}

V_{out}



V_{DD}

V_{out}

V_{DD}

V_{out}

CONCLUSION

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE Trans. Power Electron.

IEEE J. Solid-State Circuit

Σ Δ

Proc. Appl. Power Electron. Conf. Expo.

IEEE Trans. Power Electron.

Proc. IEEE Eur. Solid-State Circuits Conf.

IEEE Trans. Power Electron.

IEEE Trans. Circuits Syst. I, Reg. Papers

Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits

Proc. IEEE Int. Symp. Circuits Syst.

IEEE Trans. Power Electron.

Proc. IEE Int. Conf. Electron Devices Solid-State Circuits

IEEE Trans. Ind. Electron.