Handshaking (Flow control) and Arbitration (Output control) Mechanism for Network on chip (NoC) Routers

Purva Dave (Shrimali), Kapil Kumawat

***Abstract*— In this article, designing and implementation a NoC router based on handshaking communication protocol and Arbitration/Output control mechanism are presented. The advent of deep sub-micron technology has recently highlighted the criticality of the on-chip interconnects. As diminishing feature sizes have led to increases in global wiring delays, Network-on-Chip (NoC) architectures are viewed as a possible solution to the wiring challenge and have recently crystallized into a significant research thrust. Both NoC performance and energy budget depend heavily on the routers' buffer resources. This paper introduces a novel unified buffer structure, called the dynamic Virtual Channel Regulator (ViChaR), which dynamically allocates Virtual Channels (VC) and buffer resources according to network traffic conditions. ViChaR maximizes throughput by dispensing a variable number of VCs on demand. ViChaR's ability to provide similar performance with half the buffer size of a generic router is of paramount importance, since this can yield total area and power savings of 30% and 34%, respectively, based on synthesized designs in 90 nm technology. This paper presents Virtual Ring Routing (VRR), a new network routing protocol that occupies a unique point in the design space. VRR is inspired by overlay routing algorithms in Distributed Hash Tables (DHTs) but it does not rely on an underlying network routing protocol. It is implemented directly on top of the link layer. VRR provides both traditional point-to-point network routing and DHT routing to the node responsible for a hash table key. It performs comparably to, or better than, the best wireless routing protocol in each experiment. VRR performs well because of its unique features: it does not require network flooding or translation between fixed identifiers and locationdependent addresses.**

***Index Terms*— Handshaking Communication Protocol, Virtual channel regulator (ViChaR), Virtual Ring Router (VRR), Arbitration/Output Control, Distributed hash Table (DHT).**

I. INTRODUCTION

Power and performance are two essential features which are corresponded with each other, produce main concerns in designing and implementation. Nowadays, very large integrated digital systems [1-4] (System on chip) may contain different components such as processor, input-output units and different types of memories. Likewise, each of these components may include different specifications such as variable bandwidth, buses and different communicative protocols. Generally, bus is utilized for interconnecting the processing elements of System on Chip (SoC). However by increasing the number of processing elements, the bus itself is transmuted into a bottleneck. To obviate this difficulty, the idea of Network on Chip (NoC) has been introduced [5]. This network can be modelled as a graph wherein nodes, processing elements and edges are the connective links of the processing elements. In the second section of this article, Virtual channel regulator and Virtual Ring Router protocols are presented. In the third section, the Handshaking mechanism and arbitration output control mechanism is presented. In this section, the structure of information packets, router function and different states of the router are analyzed. In this routing, handshaking communicative protocol is utilized to interconnect different processing elements. The utilized topology for implementation is a 3×3 regular two dimensional mesh. This topology is shown in Fig. 1 shows a NoC. The features which are shown in rectangles represent NoC routers and those which are shown in circles represent the processing elements (pe) of this network.

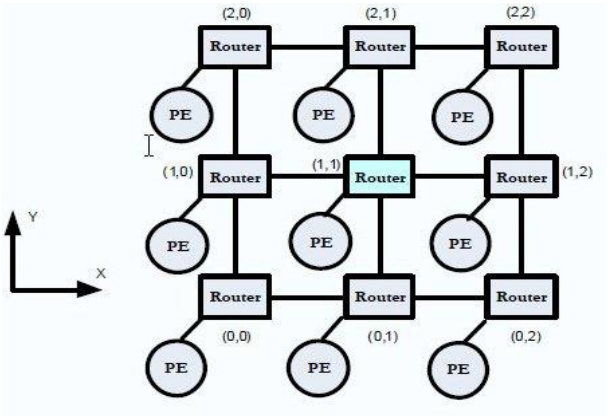

Fig. 1. A regular 3×3 mesh topology

II. DIFFERENT ROUTING PROTOCOLS

A. Virtual Channel Regulator (ViChaR): The advent of deep sub-micron technology has recently highlighted the criticality of the on-chip interconnects. As diminishing feature sizes have led to increases in global wiring delays, networkon-chip (NoC) architectures are viewed as a possible solution to the wiring challenge and have recently crystallized into a significant research thrust. Both NoC performance and energy budget depend heavily on the routers' buffer resources.

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Purva Dave (Shrimali), Department of Electronics and Telecommunication (SBCET, Jaipur RTU KOTA), INDIA
Kapil Kumawat, Department of Electronics and Telecommunication (SBCET, Jaipur RTU KOTA), INDIA

This paper introduces a novel unified buffer structure, called the dynamic virtual channel regulator (ViChaR), which dynamically allocates virtual channels (VC) and buffer resources according to network traffic conditions. ViChaR maximizes throughput by dispensing a variable number of VCs on demand. Simulation results using a cycle-accurate simulator show a performance increase of 25% on average over an equal-size generic router buffer, or similar performance using a 50% smaller buffer. ViChaR's ability to provide similar performance with half the buffer size of a generic router is of paramount importance, since this can yield total area and power savings of 30% and 34%, respectively, based on synthesized designs in 90 nm technology. Rapidly diminishing feature sizes into the nanoscale regime have resulted in dramatic increases in transistor densities. While gate delays are scaling down accordingly, wiring delays are, in fact, increasing; as wire cross-sections decrease, resistance increases. This undesirable behaviour has transformed the interconnect into a major hindrance. A signal would require multiple clock cycles to traverse the length of a large Systemon- Chip (SoC). To combat the delay issues emanating from slow global wiring, researchers have proposed the use of packet-based communication networks, known as Networkson-Chip (NoC). NoCs, much like macro networks, can scale

efficiently as the number of nodes (i.e. processing elements) increases. Besides performance, current designs indicate an additional alarming trend pertaining to the on-chip interconnects: the chip area and power budgets are increasingly being dominated by the interconnection network. As the architectural focus shifts from monolithic, computation centric designs to multi-core, communication-centric systems, communication power has become comparable to logic and memory power, and is expected to eventually surpass them. This ominous trend has been observed by several researchers and the realization of its ramifications has fuelled momentum in investigating NoC architectures. Researchers have proposed sophisticated router architectures with performance enhancements, area-constrained methodologies, powerefficient and thermal-aware designs, and fault-tolerant mechanisms. It is known that router buffers are instrumental in the overall operation of the on-chip network. However, of the different components comprising the interconnection fabric of SoCs, buffers are the largest leakage power consumers in an NoC router, consuming about 64% of the total router leakage power. Similarly, buffers consume significant dynamic power and this consumption increases rapidly as packet flow throughput increases. In fact, it has been observed that storing a packet in a buffer consumes far more energy than transmitting the packet. Furthermore, the area occupied by an on-chip router is dominated by the buffers. Consequently, buffer design plays a crucial role in architecting high performance and energy efficient on-chip interconnects.

B. Virtual Ring Routing is a novel network routing protocol that provides both point-to-point routing. VRR routes using only fixed location independent identifiers that determine. The positions of nodes in a virtual ring. Each node maintains a small number of paths proactively to its neighbours in the virtual ring. These paths can be used to forward messages between any pair of nodes and they can be set up and maintained without flooding. In this paper, we evaluated VRR in the context of ad hoc wireless networks.. The results demonstrate that VRR provides robust performance across a range of different environments and workloads. We believe that VRR could be used to route in other types of networks, for example, in enterprise networks or even in the Internet.

C. A distributed hash table (DHT) is a class of a decentralized distributed system that provides a lookup service similar to a hash table; (key, value) pairs are stored in a DHT, and any participating node can efficiently retrieve the value associated with a given key. Responsibility for maintaining the mapping from keys to values is distributed

among the nodes, in such a way that a change in the set of participants causes a minimal amount of disruption. This allows a DHT to scale to extremely large numbers of nodes and to handle continual node arrivals, departures, and failures.

VRR performs well over a wide range of wireless environments and workloads. The simulation results show that VRR achieves low delays and good delivery ratios in all experiments. The other protocols perform well in experiments but poorly in others. It is particularly interesting that VRR can achieve lower delays because it inflates the length of routing paths relative to the shortest paths discovered by the other protocols. It can achieve this because it can route around failures without waiting for routes to be repaired, and because it can repair v set-paths efficiently.

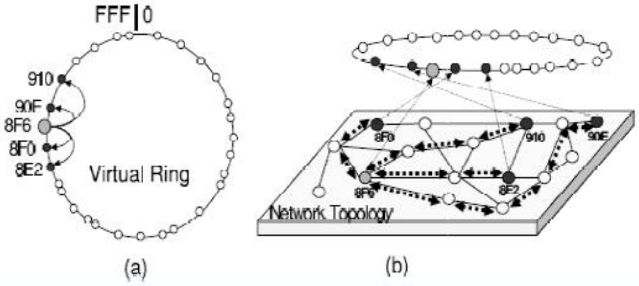

Fig.2. Relationship between the virtual ring and the physical Network topology

Refer to Figure 2, which shows all external signals for the router and describes the signals, respectively. Each unidirectional channel contains a 64-bit data portion and two control signals, send (s) and ready (r), for handshaking. There are three input channels: 1 for the processing element (pe), 1 for the clockwise (cw) direction, and 1 for the counter-clockwise (ccw) direction. Similarly there are three output channels with corresponding designations. The router is a clocked (synchronous) device, so there is also a clock input. The reset is assumed to be synchronous and asserted high. When asserted, the reset signal should initialize all state machines to their idle states and buffer statuses to empty. There is also a polarity signal output which simply indicates if the current clock cycle of the router is odd or even and is used to indicate which virtual channel is being forwarded internally for the current cycle, with the opposite virtual channel being forwarded externally for any clk cycle.

III. Flow control/ Handshaking and Arbitration /output control Mechanism

A. Flow Control/Handshaking

Since the network and routers are using fixed-size single-phit packets and each input buffer contains enough space to hold an entire packet, flow control is fairly simple. The only complexity arises from the virtual channel multiplexing. The virtual channel polarity is defined very simply based on whether the current clk cycle is even or odd. So the implication is that a router must contain some ability to track this information, e.g., a toggle function that runs continuously. By definition of this router, this cycle polarity is reset to 0 when the reset input is asserted, indicating an even cycle during reset, and after the first rising clk edge after reset is negated will toggle so that the first full clk cycle after reset is negated will be an odd cycle, with polarity equal to 1. To make the virtual channel implementation as simple as possible, the router supports both input and output buffering where every input and output virtual channel contains exactly one 64-bit packet buffer, as indicated in Figure 3. With this scheme, the following convention is assumed. On even clk cycles, packets in even input virtual channels are forwarded to even output virtual channels assuming they are granted, and any packet in an odd output virtual channel is forwarded to the corresponding odd input virtual channel of the next router, assuming the next router indicates it has space. Conversely, on clk odd cycles, packets in odd input virtual channels are forwarded to odd output virtual channels assuming they are granted, and any packet in a even output virtual channel is forwarded to the corresponding even input virtual channel of the next router, assuming the next router indicates it has space. With that definition, the virtual channels can simply be regarded as buffers that are sharing all control logic and physical wires, with even channels acted upon by the internal logic on even clk cycles and external logic on odd clk cycles, and the converse for odd channels. Furthermore, if a packet is injected on an even virtual channel through a pe port, it traverses even virtual channels for its entire traversal from source to destination, similarly for odd virtual channels. The channel synchronization signals used for handshaking are send (s) and ready (r). At system reset, all so signals should be negated (reset to 0) and ri signals should be asserted (set to 1). An input channel controller asserts that it has available buffer space by asserting its associated ri signal which is connected to the corresponding ro signal of an adjacent router. The ri signal can then simply be regarded as an indication of whether the corresponding input buffer is occupied or not. When an output channel has data that it wishes to forward and if its ro

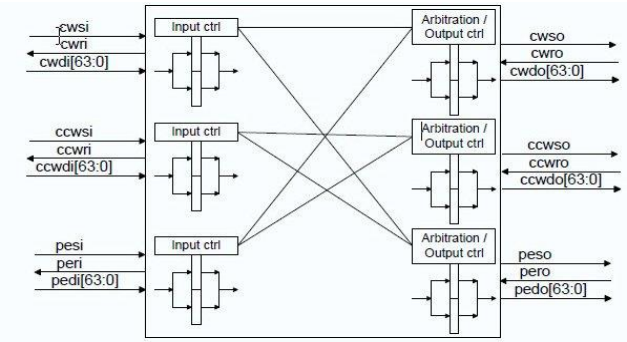

Fig. 3. Victory Router Internal Components and Switching

input signal is asserted, it asserts it's so signal along with placing the packet on the data channel. At an input channel, when a si input is asserted, on the next rising clock edge the corresponding data on the channel should be clocked into the appropriate input virtual channel buffer, depending on the polarity of the clock, as described above. During the clock cycle following the latching clock edge of the packet into a virtual channel, the input channel routing logic will decode the routing header and request the appropriate output channel. If the output channel is able to grant access to this requesting input channel (e.g., the requested output channel is not occupied and there is no contention or the requesting input channel has arbitration priority), the data is forwarded from the input virtual channel buffer to the appropriate output virtual channel buffer. Then at the next rising clock edge, the ri of the input virtual channel that was granted access to its requested output virtual channel will reassert to indicate it is ready to accept new data. An example handshaking timing diagram depicting the handshaking and timing of a packet traversal through two routers is shown in Figure 4 for this non-blocking case. A shorthand notation is used where _1 signals are associated with one router and _2 signals correspond to an adjacent router. In our case these signals could be associated with either a cw or ccw type channel or even the pe channel for the _1 input channel. (Each signal transition in Figure 4 is shown slightly delayed from a clock edge just to depict that the clock edge is a triggering event.) The diagram shows the timing for both a case when a packet is traversing even virtual channels and another case where a packet is traversing odd virtual channels. [11]

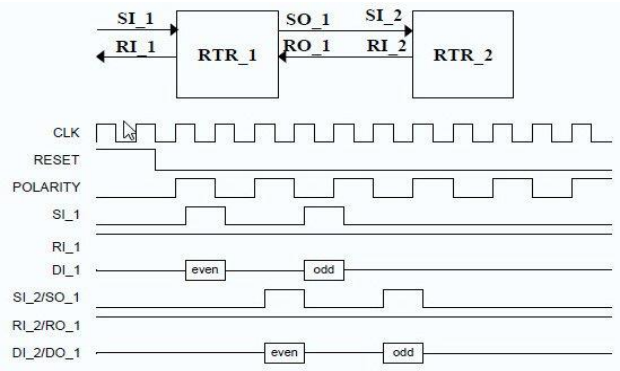

Fig. 4. Sample Handshaking Timing Diagram

Note that the output controller / arbitration logic is based on a Mealy state machine where outputs, such as so and internal grant signals to input controllers, are functions not only of the current state but also of signals, such as ro and internal request signals from input controllers. This is necessary to achieve the contention-free latency goal of a packet phit traversing one router in two clock cycles (one cycle for internal forwarding from an input channel buffer to an output channel buffer and one cycle for external forwarding from the output channel buffer to the corresponding input channel buffer of the next router).

In blocking situations, the ro signal input of an output controller will be negated. In such a case, if the output controller has data in an output buffer to forward, it must wait until the ro signal asserts before it can forward the data. Figure 6 shows the behaviour of handshaking signals for a case where an output channel of router_1 is temporarily

blocked. Similarly, blocking situations can occur internally in the router when the output channel buffer requested by an input channel buffer is currently occupied.

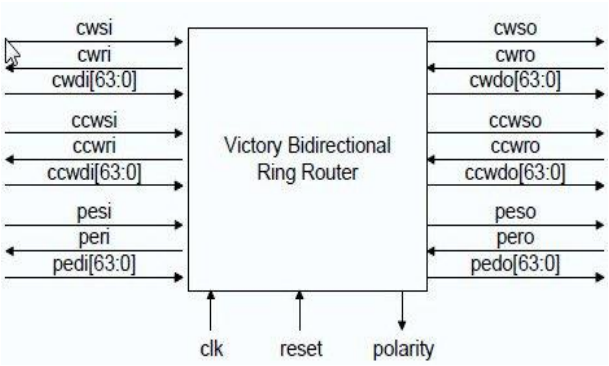

Fig. 5. Victory Router External Interface

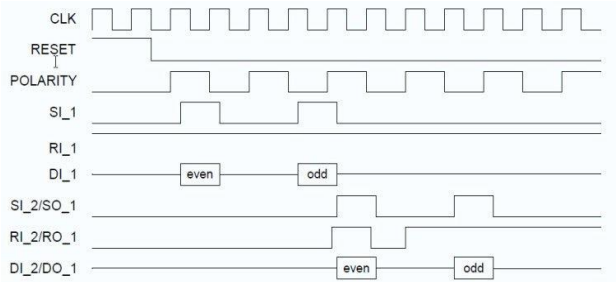

Fig. 6. Handshaking in the Case of Blocking

B. Arbitration/Output Control

A rotating arbitration scheme should be used for arbitrating among multiple requestors for each set of output virtual channels. For example, for the pe output channel of a router, there are two potential input channel buffer requestors: cw, ccw. If at the first time the pe output channel is requested after system reset there are multiple requestors, the channel should be granted to the requestor with highest priority according to the ranking cw, ccw. Once that request is granted, the output controller should log which requestor was granted and reverse the priority scheme so that the other requestor is given priority the next time the same conflict occurs. For example, if cw was the highest priority requestor the prior time the channel was granted, the new ranking for the next request becomes ccw, cw. Since virtual channels are independent, a copy of this priority tracking logic will need to be maintained for each output virtual channel. Similarly, for the cw output, the initial priority order is cw, pe; and for the ccw output, the initial priority order is ccw, pe. Note that as long as there are not multiple requests, the priority ranking is irrelevant and doesn't change. The priority ranking changes only when multiple requests conflict and the highest-priority request is granted. Arbiter is used in Network-on-Chip (NoC) router when number of input ports requested is the same as output ports. If many inputs are requested for same output port, the matrix arbiter deals it by forming a 5×5 matrix based on input and output ports. Next, it allots the priority to the requested input ports and simultaneously generates a control signal for selecting the input port to send the packet to output port. The Robin arbiter generates the grant signal on the basis of priority allotted to the input ports. [12]

Note also that regardless of how many input channel buffers are requesting a particular output channel buffer, the output channel controller can only grant access if its corresponding buffer is not occupied. Also, when a cw or ccw input channel buffer contents is being forwarded to any output buffer, note that the header portion of the packet must be manipulated (decrementing of hop count field), while all other packet info passes through unmodified. [11]

C. Channel Buffer Design

Any channel buffer can simply be implemented as a 64-bit register with a synchronous write port and a read port. Assume that writes occur on the rising edge of the clock. For input channel buffers, when the corresponding si signal is asserted, the corresponding data should be latched directly into the appropriate input channel buffer at the rising clk edge, with no computation being performed. Address decoding and output channel buffer requesting will occur on the next cycle when router internal forwarding occurs. There is no requirement for any buffer output to go into a tri-state mode. In fact, the buffer can be designed without a read enable signal such that in every clock cycle the buffer contents are available at the buffer output. Note that much of the control logic of the router depends on the status of either input or output buffers, so the implication is that every buffer has some corresponding full/empty bit or similar status tracking information.

CONCLUSION

In engineering design, always analyze the loss for each option for each optimum solution is needed. Nowadays, in very integrated digital systems, power and performance correspond closely to each other. One of the features, which directly influence on power, is the communication issue in NoCs. In this paper, design and implementation of an NoC router are analyzed. We have used an asynchronous communication mechanism based on handshaking to transfer information which implies low power consumption and scalability features. This study presents an arbitration analyses for router architecture of NoCs. The implantation of Round Robin Arbiter for the router architecture on front-end design on FPGA chip has the advantage of easy implementation and reconfigurable nature. We have also analysed for different protocols.

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[11] http://www.isi.edu/~draper/papers/vlsi04.pdf

[12] http://www.isi.edu/~draper/papers/mwscas2000.pdf