International Journal of Engineering Research And Management (IJERM)
ISSN : 2349- 2058, Volume-02, Issue-04, April 2015

Dynamic Power Reduction of SRAM memory

Isha Gautam

***Abstract*— Low power static-random access memories (SRAM) has become a critical component in modern VLSI systems. In cells, the bit-lines are the most power consuming components because of larger power dissipation in driving long bit-line with large capacitance. The cache write consumes considerable large power due to full voltage swing on the bit-line. The aim of the paper is to propose a new SRAM cell architecture to reduce the power consumption during write 0 and write 1 operation. The paper proposes a SRAM cell to reduce the power in write "0" as well as write "1"operation by introducing two tail transistors The proposed SRAM cell consumes less power than the conventional SRAM cell during write operation. The write access delay is reported to be lower than conventional. The Proposed SRAM cell designed and implemented with using .012µm CMOS technology. Simulation is performed by Microwind 3.1 & DSCH2 software. We design a 64-bits memory with the help of Proposed SRAM cell and finally the results are compared with Conventional 6T**

SRAM 64-bit memory. The power dissipated in Proposed SRAM memory is reduced up to18.88% in comparison to Conventional SRAM memory.

***Index Terms*— CMOS, Dynamic Power, SRAM, Threshold Voltage, leakage current, VLSI**

I. INTRODUCTION

Power consumption in SRAM cell is considered one of the most important problems on high performance chips due the popularity of battery operated electronic devices and mobile devices. According to research done, the power dissipated in the bit lines represents about 68% of total dynamic power consumption during a write operation only.

Therefore, most of the research work is focuses on the power reduction during write operation. For reducing the power consumption in SRAM cell, different kinds of architectures from 5-transistor to 17-transistor for Proposed SRAM cell was given in different papers. One of the oldest techniques is Zero- Aware (ZA) asymmetric Cell for reducing the dynamic power consumption. Another method is Low power 7T SRAM Cell for reducing the static power dissipation. Since, most power consumption comes from discharging of the bit lines; a 5T cell utilizing a single bit line for read/write operation has also been designed. Another common method is to use boosted word line technique to improve the write operation, however this incurs external circuitry and cell instability. Virtual grounding is a well-known technique to reduce the WRITE power consumption. The cells are based on the Vt-control of the cross-coupled inverters of the SRAM cell to reduce leakage power when SRAM is in the idle mode. The other technique is Low Power SRAM Design using Charge Sharing Technique. In this method a low-power write scheme by adopting charge sharing technique. By reducing the bit-lines voltage swing, the bit-lines dynamic power is reduced. Another method is hierarchical divided bit-line approach for reducing active power in SRAMs by reducing bit-line capacitance. During read or write mode at least one of the tail transistor must be turned OFF to disconnect the driving path of respective inverters. These transistors also reduce the sub threshold current during transistor OFF condition.

Manuscript received April 22, 2015

Isha Gautam, E & C Department, Vadodara Institute Of Engineering ,Vadodara,India

II. CONVENTIONAL 5T SRAM CELL

Figure 1 shows the schematics of conventional SRAM cell.
WRITE CYCLE. Values 1 or 0 must be placed on *Bit Line*, and the data inverted value on *~Bit Line*. Then the selection *Word Line* goes to 1. The two-inverter latch takes the *Bit Line* value. When the selection *Word Line* returns to 0, the RAM is in a memory state.
READ CYCLE. The selection signal *Word Line* must be asserted, but no information should be imposed on the bit lines. In that case, the stored data value propagates to *Bit Line*, and its inverted value
Data propagates to *~Bit Line*

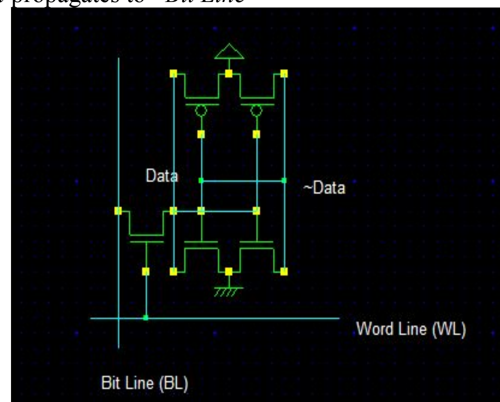
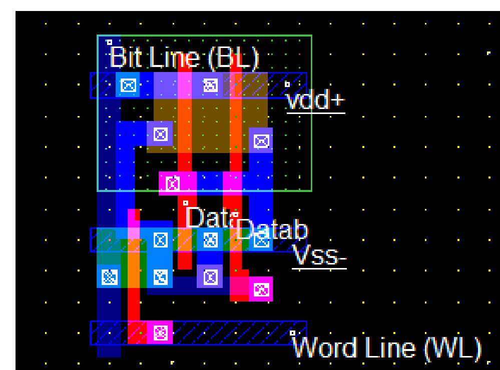


Figure 1: Design **of 5T SRAM Cell**



Fgure 2: Design of **5T SRAM Cell** (MICROWIND3.1)

SIMULATION. The simulation parameters correspond to the read and write cycle in the RAM. The proposed simulation steps consist in writing a 0, a 1, and then reading the 1. In a second phase, we write a 1, a 0, and read the 0. The *Bit Line* and *~Bit Line* signals are controlled by pulses. The floating state is obtained by inserting the letter "x" instead of 1 or 0 in the description of the signal.

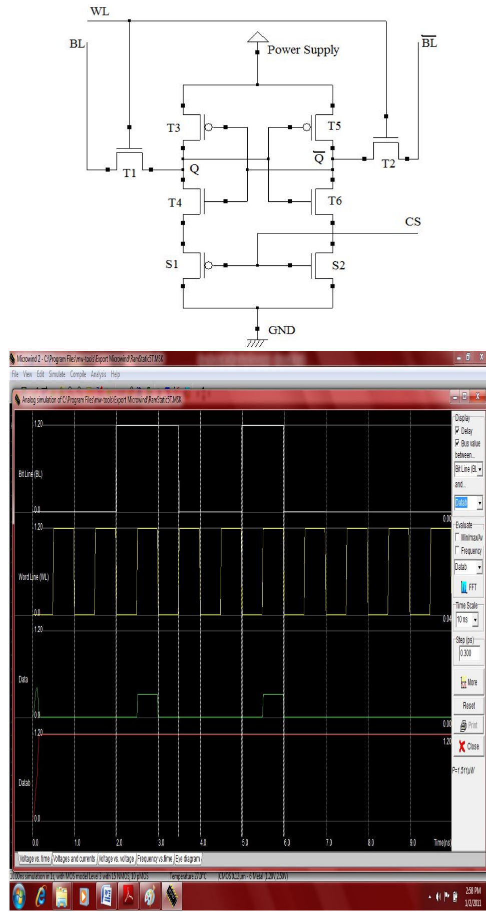


Figure 3: Simulation of a **5T SRAM Cell** (Microwind3.1)

III. PROPOSED SRAM

At time 0.0, *Data* reaches an unpredictable value of 1, after an unstable period. Meanwhile, *~Data* reaches 0. At time 0.5ns, the memory cell is selected by a 1 on *Word Line*. As the *Bit Line* information is 0, the memory
Cell information *Data* goes down to 0. At time 1.5ns, the memory cell is selected again. As the *Bit Line* information is now 1, the memory cell information *Data* goes to 1. During the read cycle, in which *Bit Line* and *~Bit Line* signals are floating, the memory sets these wires respectively to 1 and 0, corresponding to the stored values
In the proposed cell we are using two more transistors S1 and S2 for reducing the power dissipation. Control Signal (CS) is used for controlling the S1 and S2 during Write "0" and write "1" operation.

3.1 Write mode

In dynamic logic circuits, the two bit-lines are pre-charged initially to power supply ( ). When the word line (WL) is high, the input data and its complement are placed on the BL and. The bit-lines are the most power consuming components in the conventional SRAM cell because of large power dissipation in driving the long bit-lines with larger capacitance. Since, write consumes considerable larger power due to the full voltage swing on the bit-lines therefore in the present paper we have given more emphasis on the write operation. We will consider two write operation in detail for our proposed SRAM cell. In our proposed cell, for write operation we will select CS as per operation. Proposed cell mainly contains 8-transistors. We will consider two write modes:

3.1.1 Write "1" mode.

In write "1" mode, node B must be written to low that can be achieved by setting BL to "0" and asserting WL. Path for write "1" operation is shown in figure 3. The two possible cases are:
3.1.1. a. Case I writing the cell state from 1 to 1. This is not possible because both node B and BL are at zero potential.
3.1.1. b. Case II writing the cell state from "0" to one (0-1). In our proposed cell, it is easy to flip the cell state from 0 to 1 by setting CS is high before asserting WL

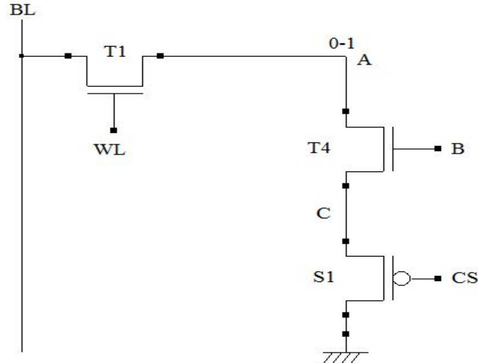


Figure 5. Path for write "1" operation

3.1.2 Write "0" mode.

In write "0" mode, the node B must be written to high that is done by setting BL to and asserting WL. Path for write "0" operation is shown in the figure 4. The two possible cases are:
3.1.2. a. Case I: Write pattern is 0 - 0, since node B is initially high therefore this write pattern is not possible.

3.1.2. b. Case II: 1 - 0. This write pattern can be easily performed in our proposed cell by setting CS is low, so that pull down path through driver transistor M2 of inv-B is disconnected. Now assert WL is high to perform the desired write pattern.

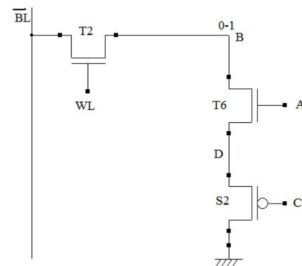


Figure 6. Path for write "0" operation

In the proposed circuit, the CS signal is used to ensure the correct operation and by selecting proper value of signal CS before asserting WL, transition from 1 - 0 and 0 - 1 can be

easily allowed. The two pull down transistor are used to reduce the Sub threshold current which is flowing in the circuit when transistor is in Cut Off region. This leakage current is dependent on Threshold Voltage. As the threshold voltage decrease the Sub-threshold current increases. Because of drain induced barrier lowering (DIBL) in the MOSFET the threshold voltage decreases as the Drain voltage increases. The use of two trail transistor is reducing the drain voltage which increases the threshold voltage. The increase in threshold voltage results in decreased sub-threshold current which reduces the power dissipation. For proper working of SRAM cell, the size of the transistors is a major factor. According to Thumb Rule, the Width ratio of T3 and T1 is nearly equal to 1.5 and the Width ratio for T1 and T4 is also equal to 1.5. Similarly it is applicable for T5, T2 and T2, T6. And This size configuration provides the proper driving voltage to transistors for ON and OFF condition.

IV. Results and Discussion

This section provides the detailed simulation analysis of the proposed SRAM cell. We estimate the impact of the proposed SRAM cell on the power dissipation during write operation. The schematic of Proposed SRAM cell is designed and implemented by using Dsch and Microwind. For simulation we are using BSim4 model with 1V power supply. The proposed design has been simulated using CMOS 90nm technology. Then we design a 64-bits memory by using Proposed SRAM cell and the result is compared with Conventional 5-T SRAM cell. The two stack transistors reduce dynamic power consumption during write operation through proper charging and discharging of the bit lines. In the conventional SRAM cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power dissipation in both write “0” and “1” is more. In our proposed SRAM cell as shown in figure 2, we are preventing any single bit line from being discharged during write “0” as well as write “1” mode by proper selection of signal CS, which turn either S1 or S2 OFF. We design a Layout of the Proposed SRAM cell by using Microwind Layout Design Tool. The Layout of proposed SRAM has been shown in figure5. The layout is based on λ- Design Rules, where λ is equal to the Half of the length of the transistor used in standard foundry that is.012µm.

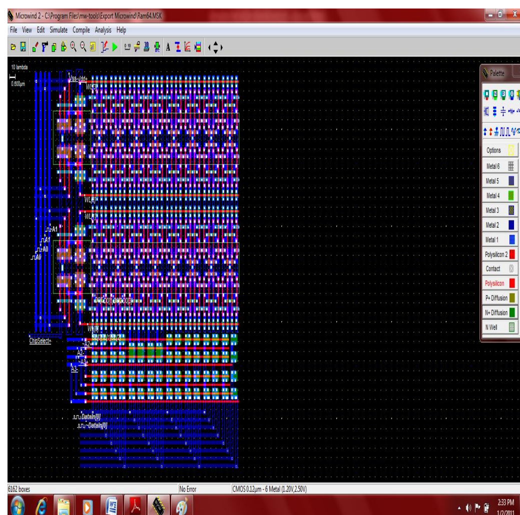


Figure 7. Layout of Proposed 64-bit SRAM cell

Figure 7 shows the analog simulation diagram of proposed SRAM cell. Simulation is performed using BSim4 Model. Simulation parameters are shown in Table I. We calculate the power dissipation during Write operation and compared the result with 6T SRAM cell. In proposed SRAM cell power consumption is reduced up to 19.83% in comparison to Conventional 6T SRAM cell.

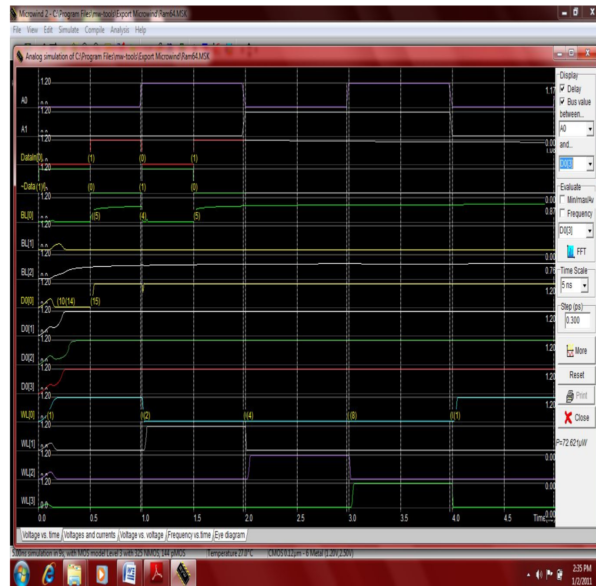


Figure 8: Simulation 64-bit SRAM cell

We have also design the 64-bit memory by using Proposed SRAM cell and finally compared the power dissipation results with 6T SRAM cell. The design of 64-bit proposed SRAM memory is shown in figure 9. From the simulation result we find that the power consumption in Proposed 64-bit SRAM memory is less than the 6T SRAM memory. Proposed SRAM memory is shown in proposed SRAM cell the crosstalk voltage values are increased for bit lines, word line (WL) and for outputs in comparison to conventional SRAM cell but these values can be controlled with the help of proper sizing of Width (W) and Length (L) of the transistor.

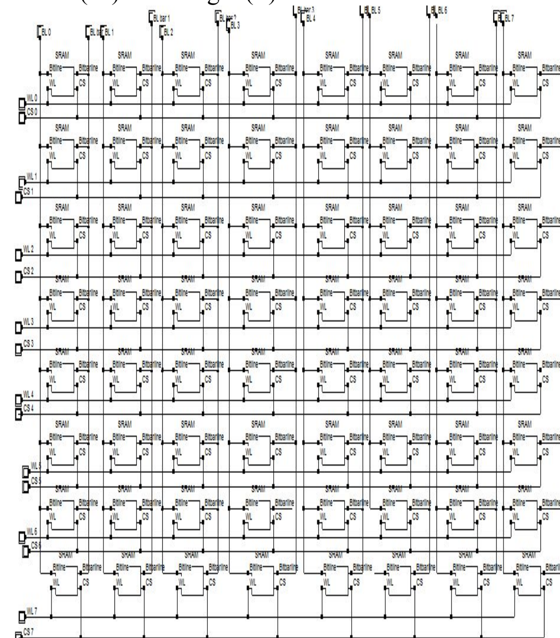


Figure: 9. 64-bits Proposed SRAM Memory Design

CONCLUSION AND FUTURE WORK

Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. But here proposed SRAM cell can reduce the power in write operation by introducing two tail Transistors in the Pulldown path for reducing leakages. Due to these Stack transistors the power dissipation has reduced up to 19.83% for a single SRAM cell and 18.88% for 64-bits memory in comparison to Conventional 6T SRAM. Although number of transistors are increased but relative power dissipation is also be reduced. In future work we will design area efficient Proposed SRAM memory with the help of Layout Design Techniques. This proposed SRAM cell can be used to provide low power and low cost solution for portable devices like laptops, mobile phones etc.

REFERENCES

[1] Moshnyaga, V. G., Inoue, K., "Low Power CacheDesign", *Low power processors and systems on chips*, *CRC Press, Florida,* pp.8-11, 2006.

[2] Yung-Do Yang and Lee-Sup Kim, "A Low-Power SRAM Using Hierarchical Bit Line and Local Sense Amplifiers" *IEEE Journal of solid state circuits*, Vol. 40, No. 6, June 2005.

[3] Sayeed A. Badrudduza, Ziyan Wang, Giby Samson and Lawerence T.Clark, "Leakage Controlled Read Stable Static Random Access Memories," *Journal of Computers*, Vol.3, no.4, pp.39-49, 2008.

[4] Ajay Kumar Singh and CMR Prabhu, "Design of low power SRAM cell for write/read operation", *Asian Journal of Physics,* Vol.17, no 2, pp. 273-278, 2008.

[5] Prabu, C.M.R. and Ajay Kumar Singh, "A proposed SRAM cell for low power consumption during write operation", Emerald Insights. *International journal of Microelectronics*, Vol.26, no. 1, pp. 37- 42, 2009.

[6] Rajiv V.Joshi, Saibal Mukhopadhyay, Donald W.Plass, Yuen H.Chan, Ching-Te Chuang and Yue Tan, "Design of Sub-90nm Low-Power and Variation Tolerant PD/SOI SRAM cell Based .