DESIGN OF OPTIMIZED DDFS FOR FPGA IMPLEMENTATION

AMRUTHA S.R, DEEKSHA.A, FAIZAN FAYAZ BHAT, POOJA.H, SANDEEP K V

***Abstract*— Direct Digital Synthesizer is a type of frequency synthesizer where arbitrary waveforms are created from a single and fixed frequency reference clock. An optimized Direct Digital frequency Synthesizer (DDFS) is designed for FPGA implementation considering the Software Defined Radio (SDR) application which makes use of Orthogonal Frequency Division Multiplexing (OFDM) technique. SDR is a radio communication system which consists of transmitter and receiver where the components implemented in a hardware is instead implemented by means of software on a personal computer or embedded system by making use of the digital signal processing (DSP) for coding, decoding, modulating and demodulating data. The structure for hardware implementation of SDR makes use of OFDM technique. The structure comprises of VLSI mapping of algorithms, OFDM, Quadrature Phase Shift Keying (QPSK), Fast Fourier Transform (FFT) Algorithms and most importantly, the algorithm for DDFS. The VLSI implementation of the DDFS can compute sine and cosine function on a single edge of a clock, thus achieving optimization in terms of area, speed and reduction in power consumption is achieved by making use of Fixed-point implementation. Verilog HDL is used as a description language for mapping Algorithms in VLSI. Xilinx Spartan3 XC3S400 Field Programmable Gate Array (FPGA) was chosen as a Hardware Platform for the System Implementation. The output can be seen in the analog form by interfacing the FPGA to a Digital to Analog converter (DAC).**

***Index Terms*— Software Defined Radio, Direct Digital Frequency Synthesis, Orthogonal Frequency Division Multiplexing, Field Programmable Gate Array, digital signal processing, Quadrature Phase Shift Keying.**

I. INTRODUCTION

A Software Defined Radio (SDR) is defined as a radio in which the receive digitization is performed at some stage downstream from the antenna, followed by wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages - with a reverse process occurring for the transmit digitization. Digital Signal Processing present in the SDR is flexible and is reconfigurable functional blocks which define the characteristics of the radio.

As technology progresses, an SDR can move to an almost total Software Radio (SR), where the digitization is at (or very near to) the antenna and all of the processing required for the radio is performed by software residing in high-speed digital signal processing elements.

The backbone of SDR structure in digital domain is the Direct Digital frequency synthesizer (DDFS).The DDFS is responsible for the generation of high frequency carrier waves in digital domain and modulating the message on it and then convert it to analog using digital to analog converter (DAC) before antenna, this section of the system is known as digital up-conversion (DUC). The counter-part of DUC on the receiver end is known as digital down-converter (DDC).

The key challenge for researchers is the optimization in terms of area as well as time. The optimization in DDFS includes two different designs namely Lookup Table and Coordinate Rotation Digital Computer (CORDIC).

II. EXISTING SYSTEM

Look up tables based designs required huge ROM's for implementation and hence were declared to be area hungry. On the other hand, CORDIC based technique used iterative algorithms for computation of sine and cosine values, hence was declared inefficient.

To overcome the issues faced in the above mentioned techniques, Singleton used basic trigonometric identities to compute sine and cosine values where each sample of sine and cosine requires 4 multiplications and 2 additions. Hence the existing system is found to be simpler and faster. It utilizes 2 adders and 2 multipliers to generate a sample of sine and cosine. The design is found to be more area and time efficient compared to CORDIC and Look-up tables based approaches. As shown in Fig 1, the architecture for VLSI implementation has utilized registers being triggered on the positive and negative edges of same clock. Such designs are not synthesizable on FPGA.

The timing diagram of sine and cosine values that are generated with respect to the system clock is shown in Fig 2, where the sine sample generated at negative edge of clock is used to generate the cosine sample at positive edge of the system clock

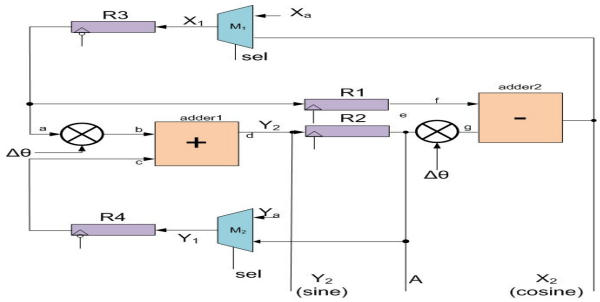

Fig 1. Existing system architecture

Manuscript received May 10, 2015

AMRUTHA S.R, Dept. of Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India

DEEKSHA.A, Dept. of Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India

FAIZAN FAYAZ BHAT, Dept. of Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India

POOJA.H, Dept. of Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India

SANDEEP K V, Assistant. Professor, Dept. of Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India

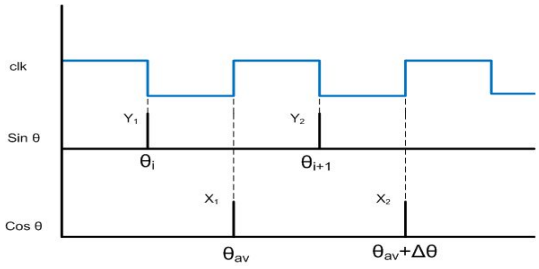

Fig 2.Timing diagram for existing system

III. PROPOSED SYSTEM

The proposed architecture makes use of two adders, two multiplexers, two multipliers and two registers. The proposed system is general and applicable to any bit length. The data path elements are 32 bits wide. As compared to the existing architecture, the required number of registers has been reduced to two, instead of four. Depending upon the number of bits used, it results in considerable reduction of hardware resources. Initially *Yi* and *Xi* are fed to the Registers because *sel* is 1. On the next positive edge of *clk*, these seed values are used to compute the values of Sine and Cosine. After the first clock cycle, *sel* is 0 and now the multiplexers only act as simple wires for rest of the clock cycles. The previous value of Cosine is multiplied by $\Delta\theta$ and added with the previous value of Sine to generate the current value of Sine, *Yc*. Similarly, the previous value of Sine, *Yp* is multiplied by $\Delta\theta$ and subtracted from the previous value of Cosine**,** *Xp* to generate the current value of Cosine, *Xc*. Additionally to the proposed system an edging clock is included and hence the reduction in power consumption can be achieved.

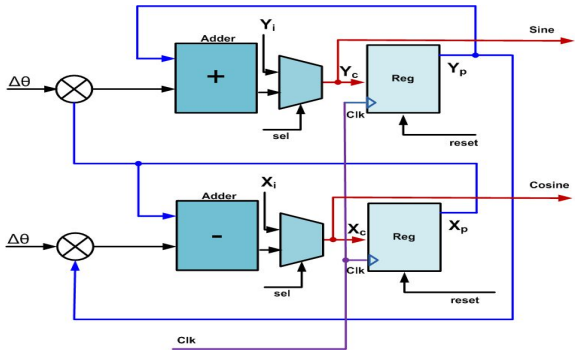

Fig 3. Proposed architecture

IV. BLOCK DIAGRAM

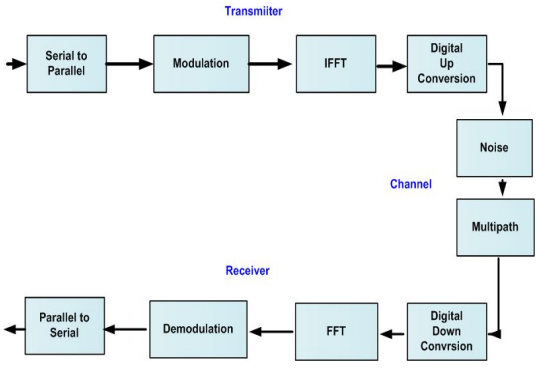

Fig 4.Block Diagram of OFDM SDR

The work contains simulation and Verilog HDL implementation of OFDM based transmitter and receiver system. After floating point simulation of the framework, Verilog HDL has been used for fixed point simulation and description of hardware details. On the transmitter side, the input which is in serial form is converted into parallel sets. For eg: if the input takes 8 bits in at a time, when passed through serial to parallel converter, 4 parallel set of two bits each is obtained. Each set of data contains one information bit for each carrier frequency. Then, parallel data obtained are made to pass through a modulator where QPSK technique is used to obtain modulated signal at orthogonal carrier frequencies. The IFFT section, then converts the parallel data into time domain waveforms.

Finally, these waveforms are passed through DUC, where the waveforms obtained are combined to form a single time domain signal for transmission. By making use of the OFDM scheme, the channel simulation will allow for us to examine the effects of noise and multipath by adding small amount of random data to the transmitted signal, simple noise can be simulated. Multipath simulation is made possible by adding attenuated and delayed copies of the transmitted signal to the original. Hence the problem in wireless communication when the signal propagates on many paths can be simulated. The receiver section basically performs the inverse of the transmitter, initially by separating the data into parallel streams. The FFT converts the parallel data streams into frequency domain data. The data are now available in modulated form on the orthogonal carriers. Demodulation down-converts this information back to the baseband. Finally, the parallel data are converted back into a serial stream to recover the original signal. The overall block diagram of the system has been shown in Fig 4.

The proposed system is made use in the Digital up converter and Digital down converter of the block diagram to achieve optimization in terms of are, speed an reduction in power consumption.

CONCLUSION

The proposed structure compared to the existing system consumes lesser silicon area and can be implemented on FPGA. This is due to the fact that it generates the sine and cosine values on a single edge of the system clock. By making use of a edging clock, reduction in power consumption is achieved. The required memory resources are extremely less as only two 32-bit registers have been used in the architecture. The future goals include the reduction of the critical path, so that the framework may work at even higher clock rate and the range of frequency generated may be increased. The further developments in the optimization may lead to ideal cognitive radio.

ACKNOWLEDGMENT

The successful completion of task would be incomplete without complementing those who made it possible and whose guidance and encouragement made our efforts successful. With deep sense of gratitude we acknowledge the help and encouragement of our guide, Mr. Sandeep K V Asst. Prof., Dept. of TCE, DSCE, Bangalore, for his successful guidance, support, help and suggestions. We would also like to express our deep sense of gratitude to Dr A R Aswatha,

Head of the Department of Telecommunication Engineering for his exemplary guidance, valuable suggestions, expert advice and encouragement. We take great pleasure in expressing our sincere thanks to Dr. A.N.N Murthy, Principal DSCE Bangalore, for his valuable support. We take this opportunity in expressing gratitude and respect to all those who directly or indirectly helped and encouraged us during the course of project.

REFERENCES

[1] W. Tuttlebee, *Software Defined Radio Enabling Technologies*. John Wiley and Sons, 2002.

[2] Y. A. Khan, Aneesullah, and H. Ali, "Differential based area Efficient rom less quadrature direct digital frequency synthesis," in *IEEE 5th International Conference on Emerging Technologies (ICET)*, pp. 83 – 88

[3] T. Zaidi, Q. Chaudry, and S. A. Khan, "An area and time efficient

[4] Collapsed modified cordic ddfs architecture for high rate digital Receivers," in *IEEE 8th International Multitopic Conference*, pp.677–681.

[5] Jyohi.N, Jayaprakash.s and Shilpa K. Gowda, "Design and VLSI implementation of High performance DUC and DDC for Software defined radio applications"

[6] Asraf Mohamed Moubark, Mohd Alauddin Mohd Ali, Sawal Hamid Md Ali, Hilmi Sanusi and Nasharuddin Zaina, "Simple QPSK Modulator Implemented in Virtex 6 FPGA Board for Satellite Ground Station"