Modern Complex RADAR signal Emulator for RADAR signal processing and testing Applications

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Abstract— **These days RADARs use complex techniques such as stagger PRI, jitter PRI with frequency agile characteristics. The frequency agile RADARs switch frequencies with in a pulse to get different types of advantages. Today lot of RADAR signal processing takes place on FPGA platform. These signal processing algorithms include pulse parameters estimation, de-interleaving of mixed pulse patterns, processing complex chirp signals etc. All these algorithms need to be tested at various levels before they get integrated into final system. The project design consists of mainly two modules; The scenario creator and the control logic. Control logic communicates with PC using serial port to capture the parameters set by the user in PC. These parameters are loaded into respective source simulator modules. Each source simulator module consists of NCO for digital carrier generation and pulse modulator. The NCO is programmable to generate all types of frequency agile signals in real time. A top level module consists of all these blocks and will be synthesized to Xilinx FPGAs. The work focuses on the digital implementation inside FPGA. The external costly DAC board is assumed to be standard and is not considered for demonstration of project. Instead, the final FPGA output which is supposed to be DAC input will be demonstrated in real-time with Chip-scope Pro software.**

Index Terms— **DDS, NCO, baseband waveform generator, Up conversion, BITE generator and FPGA**

I. INTRODUCTION

Radar parametric testing has traditionally required either expensive trials in real-world situations (with many uncontrolled variables) or very limited 'canned' tests. The Von Neumann processors normally used for signal processing are severely limited in this application because of the inherently serial instruction stream. This paper gives the use of FPGAs to the processing to obtain a near real-time environment simulator. The FPGA logic handles the time sensitive tasks such as target sorting, waveform generation, sea clutter modeling and noise generation. DSP microprocessors handle the less critical tasks like target movement and radar platform motion. The result is a simulator that simultaneously produces several hundred independent moving targets, realistic sea clutter, land masses, weather, jammers and receiver noise. Traditional Radar Target Generators are built to test, debug, and demonstrate radar and target tracking functions. The aim is to perform some basic testing. The number of targets is limited and target motion is simple. The radar platform doesn't change position or attitude. Interference is simulated by a simple Gaussian noise generator. The test scenarios are canned; there is no real time interaction between the radar/operator and the Emulator. The Radar Environment Simulator is controlled by, and is partially implemented in software. Tasks that are not time critical are handled by software.

Time critical tasks are performed by custom hardware. The term "radar" is generally understood to mean a method by means of which short electromagnetic waves are used to detect distant objects and determine their location and movement. The term RADAR is an acronym from **RA**dio **D**etection **A**nd **R**anging. A complete radar measuring system is comprised of a transmitter with antenna, a transmission path, the reflecting target, a further transmission path (usually identical with the first one), and a receiver with antenna. Two separate antennas may be used, but often just one is used for both transmitting and receiving the radar signal. Radar is an electromagnetic system for the detection and location of objects. It operates by transmitting a particular type of waveform, a pulse-modulated sine wave for example, and detects the nature of the echo signal. Radar is used to extend the capabilities of ones senses for observing the environment, especially the sense of vision. The value of radar lies not in being a substitute for the eye, but in doing what the eye cannot do. Radar cannot resolve detail as well as the eye, nor is it capable of recognizing the "color" of objects to the degree of sophistication of which the eye is capable. However the radar can be designed to see through those conditions impervious to normal human vision such as darkness, haze, fog, rain, and snow. In addition the radar is having the advantage of being able to measure the distance or range of the object. This is probably the most important attribute.

An elementary form of radar consists of a transmitting antenna emitting electromagnetic radiation generated by an oscillator of some sort, a receiving antenna, and an energy-detecting device, or receiver. A portion of the transmitted signal is intercepted by a reflecting object (target) and is reradiated in all directions. It is the energy eradiated in the back direction that is of prime interest to the radar. The receiving antenna collects the returned energy and delivers it to a receiver, where it is processed to detect the presence of the target and to extract its location and relative velocity. The distance to the target is determined by measuring the time taken for the radar signal to travel to the target and back. The direction, or angular position, of the target may be determined from the direction of arrival of the reflected wave-front. The usual method of measuring the direction of arrival is with

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narrow antenna beams. If relative motion exists between target and radar, the shift in the carrier frequency of the reflected wave (Doppler Effect) is the measure of the targets relative (radial) velocity and may be used to distinguish moving targets from stationary objects. In radars which continuously track the movement of the target, a continuous indication of the rate of change of target position is also available. It was first developed as a detection device to warn of the approach of hostile aircraft and for detecting antiaircraft weapons. Although well-designed modern radar can usually extract more information from the target signal than merely range, the measurement of range is still one of radar's most important functions. There seem to be no other competitive techniques which can measure range as well as or as rapidly as can a radar.

II. AVAILABLE METHODS

Radar Emulator is the technique used test the various techniques or methodologies being developed for RADAR systems which can be tested without being cost-effective realistic radar systems. The simulators have been developed for scholars or researchers in the field of Radar processing for its high performance to test its signal processing applications at software level to implements new ideas and method as far as the modulation schemes utilized. But at these simulators intended user may not get as précised output results and need to have a special system which replaces the following:

i) The output results as close to the practical values of realistic radar system and

ii) Rapid development platform for emulator and cost effective.

III. METHOD PROPOSED

The Field Programmable Gate Array are used in the place of traditional ASIC's which stands for Application Specific Integrated Circuits used in developing new systems or application based devices. By these programmable devices the user can make the device (FPGA here) optimized to their précised level so as to make the emulation nearest to the practical one. The performance of Radar systems can greatly influenced by their mechanical design and modern digital modulation schemes. Here the other is chosen because the later one to that is an emulator platform for Radar to test different modulation schemes as like realistic radar based system in which FPGA is used. The flow chart for the total flow can be illustrated in the form a diagram as shown below.

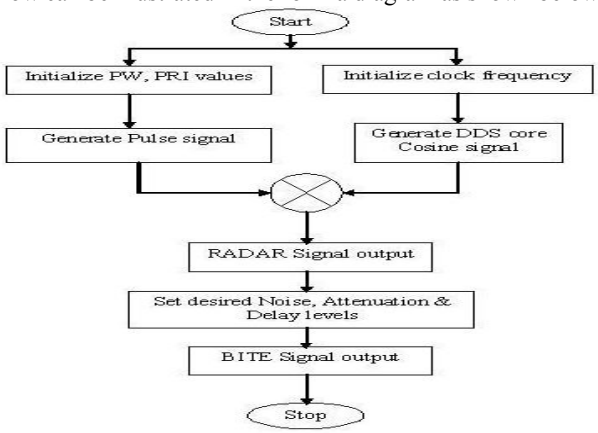

Fig1: Flow chart of design flow

The Field Programmable Gate Array has been taken because of the following signal processing algorithm issues:

1) Pulse parameters estimation
2) De interleaving of mixed pulse pattern
3) Processing complex pseudo signals etc.

A. Block Diagram

The following diagram shows the simplified description of the RADAR Emulator Implemented on single FPGA board and for demonstration purpose PC is used. The functional modules will be discussed in detail in the following chapter and all the major blocks expect DDS (Direct Digital Synthesizer) has implanted by IP Core from Xilinx core generator tool and remaining are using VHDL. External control switches from FPGA development board has been used to get different combinations of frequency and an attenuation variation which resembles the phase and noise as added to original received echo signal from target as viewed in RADAR.

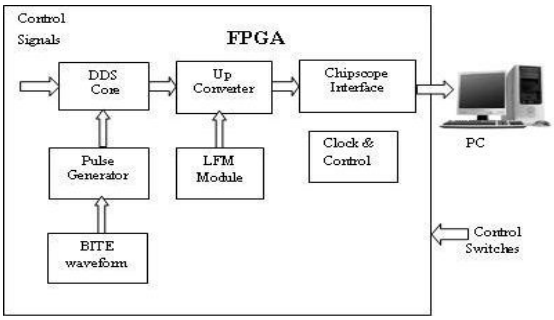

Fig2: Functional overview of RADAR emulator implemented on FPGA

B. Timing generator and Encoder interface

The encoder interface gets input from radar antenna and it will generate the timing signals of radar as per the antenna rotation. As a test case design the encoder considered here is one, which provides serial data in gray format at its output. the encoder interface implemented on the FPGA generates 17 clock pulses at the frequency of 400 kHz at regular intervals. These clock pulses along with proper direction and control enables are sent to the external encoder. the encoder puts data serially at the rising edge of each 17-clock pulse. FPGA performs the operation of serial to parallel conversion and gray to binary conversion of the valid bits of the received data. The error checking of the data received is also done at the FPGA.

C. Waveform coefficient generation

The waveform coefficients are computed and stored in the ROMs of the FPGA. In this design, the linear frequency modulation for the waveform is considered. Frequency or phase-modulated waveforms can be used to achieve much wider operating bandwidths. Linear Frequency Modulation (LFM) is most commonly used. Here, the frequency is swept linearly across the pulse width, either upward (up-chirp) or downward (down-chirp). The LFM up-chirp instantaneous phase can be expressed by $\Psi(t) = 2*\Pi*(f0 * t + \mu * t2/2) - \tau/2 \le t \le \tau/2$ where f0 is the radar center frequency, and $\mu=2\Pi$ B/t is the LFM coefficient. Thus, the instantaneous frequency is $f(t) = (1/2*\Pi)* d/dt (\Psi(t))= f0 + \mu * t - \tau/2 \le t \le \tau/2$ Similarly, the down-chirp instantaneous frequency is given by f(t)=

$(1/2*\Pi)* d/dt (\Psi(t))= f0 - \mu * t - \tau/2 \leq t \leq \tau/2$ The linear frequency modulation coefficients are computed as per above equations. The sampling frequency is chosen corresponding to the bandwidth of the waveform to be generated. These coefficients are computed offline for different pulse widths and stored into the ROMs of the FPGA. In real time these coefficients are read in the FPGA to generate LFM waveform at IF.

D. Up conversion of frequency modulated waveform to IF

Fig. shows the design schematics of up-conversion (to IF) module as implemented in FPGA. CPI, BITE, PRT signals form the input to the module along with the clock. These are the timing signals, which are generated in the FPGA from the external encoder data. CPI is used to synchronize the modulated waveform with the radar timings. PRT acts as the cover pulse of the transmission waveform and is used to enable the DDS (Direct Digital Synthesizer) implemented in the FPGA.

When enabled the DDS generates continuous wave signal at the IF at which LFM is to be generated. For the design under consideration the IF is 40 MHz So the DDS generates continuous wave at 40 MHz during the PRT. The complex continuous waveform at the output of the DDS is then multiplied with the LFM coefficients (at baseband) already stored in the ROM of the FPGA. There are two banks of ROMs, one for cosine LFM coefficients and other for sine LFM coefficients. The user from the display selects the pulse width for which LFM is to be generated and the information is conveyed to the FPGA. According to the pulse width selected, the selection of ROM is done and the LFM coefficients are read out in real time to form the LFM waveform at IF. Accordingly, the ROM selection bits are set and address generation is done to read the coefficients from the ROM. After multiplication of the cosine and sine components of the continuous signal at IF with corresponding LFM coefficients, the signal at the output of the multipliers is subtracted to from the linear frequency modulated signal at the IF. The signal is then filtered by a band pass filter implemented in the FPGA so as to remove the out of band components. The digital LFM signal thus generated is with zero Doppler. The digital LFM signal (at the IF) at the output of the FPGA is then fed to an external Digital to Analog Converter (DAC) followed by an analog filter. The signal is then up converted to the desired transmission frequency by RF up converters and transmitted during the PRT pulse. Fig. : Baseband waveform generation and up conversion to IF.

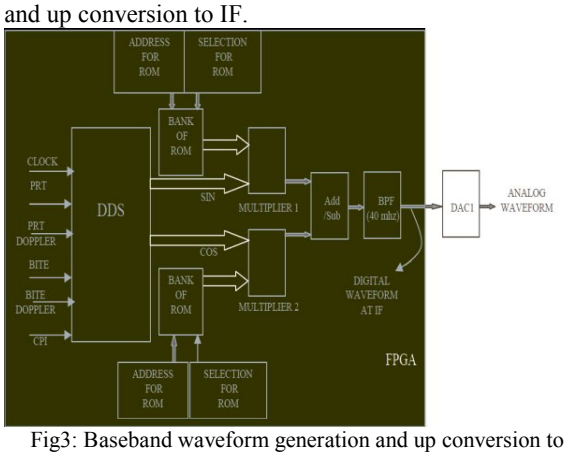

Fig3: Baseband waveform generation and up conversion to IF

The Modulated version of the transmit waveform is shown below.

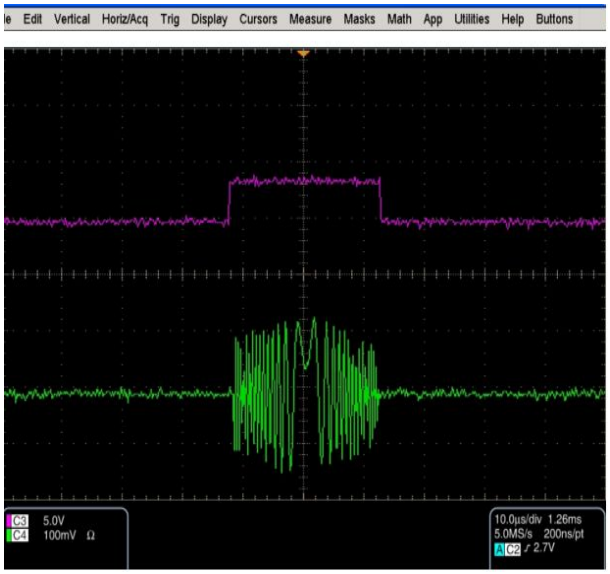

Fig4: Modulated transmit waveform as Generated by FPGA

E. BITE waveform generation

BITE is used to check the essential functionalities of the radar when it's not transmitting. It acts as the echo return from real targets. The design is capable of generating BITEs with and without Doppler i.e. moving as well as stationary targets can be simulated. Along with BITE, BITE Doppler also forms an input to the DDS. The signal BITE enables the DDS for the range position during which the echo is to be simulated and thus acts as the cover pulse for the BITE to be generated. BITE position and Doppler of the BITE are programmable by the user. The maximum Doppler for which the BITE can be generated depends on the PRF chosen by the user and is equal to PRF/2. Once the Doppler value and the BITE position have been fed to the DDS, the DDS generates the continuous wave at the corresponding frequency (depending on the Doppler input). The cosine and sine components of this signal are then multiplied with the corresponding LFM coefficients as read from the ROM (selected as per pulse width) and then the same process of upconversion follows. For ground-based radars, the waveform is always transmitted with zero Doppler and the waveform generation process adopted is explained above. Depending on the Doppler of the received echo, information about Doppler and speed of the target is ascertained and used for further processing. For radars on moving platform, an inherent Doppler gets introduced due to movement of the radar. This leads to ambiguity in Doppler measurement of the received echo. Further this gives rise to poor clutter cancellation in the radar. Thus, it is essential for moving radars to nullify the effect of the Doppler that come into picture due to their own movement. This could be undertaken either in the Digital Down Conversion (DDC) stage in the receiver signal processor or, for a relatively slow moving platform like a ship, in the transmission stage itself. The assumption here is that within a dwell period there is no significant change of Doppler. The waveform generated can be shifted by an amount equal to the Doppler of the platform in a particular such that returns from a stationary target will come with zero Doppler.

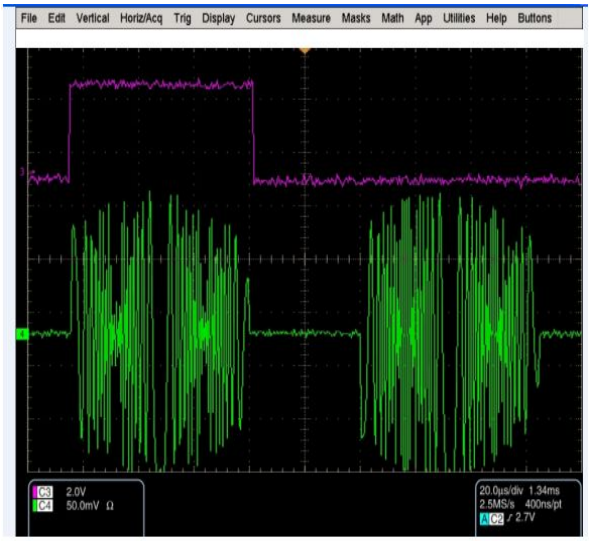

Fig5: Transmit & BITE waveform at output of FPGA

F. DDS core

Function generators have been around for a long while. Over time, these instruments have accumulated a long list of features. Starting with just a few knobs for setting the amplitude and frequency of a sinusoidal output, function generators now provide wider frequency ranges, calibrated output levels, a variety of waveforms, modulation modes, computer interfaces, and in some cases, arbitrary functions. The many features added to function generators have complicated their design and increased their cost. There is an opportunity for a radical re-design of the familiar function generator using direct digital synthesis (DDS) provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation. These features which were 'tacked-on' to function generators now are handled in a clean, fundamental way by DDS. Fig. shows the DDS core architecture.

The Logi CORE™ IP DDS (Direct Digital Synthesizer) Compiler core sources sinusoidal waveforms for use in many applications. A DDS consists of a Phase Generator and a SIN/COS Lookup Table. These parts are available individually or combined via this core. Direct digital synthesis (DDS) is a method of producing an analog waveform, usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to- analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

G. Sin/Cos LUT

When configured as a Sin/Cos LUT, the Phase Generator is not implemented, and the phase is input via the PHASE_IN port, and transformed into the sine and cosine outputs using a look-up table. Efficient memory usage is achieved using half wave and quarter wave storage schemes. The presence of both outputs and their negation are configurable when the core is customized. Precision can be increased using optional Taylor Series Correction. This exploits Extreme DSP slices on FPGA families that support them to achieve high SFDR with high speed operation.

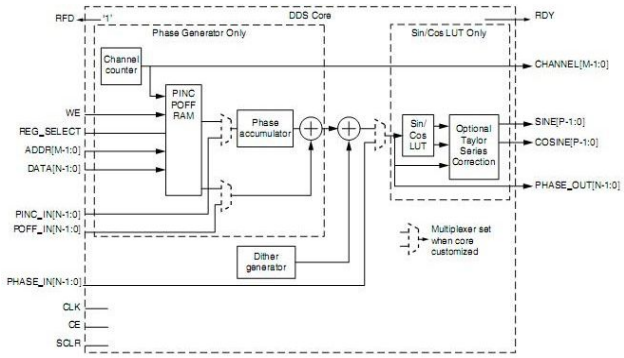

Fig6: DDS Compiler core

The output of the FPGA is fed to a digital to analog converter to get the analog transmission waveform at IF. Different modulation types can be stored in the external memory and loaded to FPGA to provide flexibility to change the modulation on the fly. This can be a significant ECCM feature for the radar. The clock frequency used in the design is of 100 MHz; the coefficients are then up sampled by 10 to get samples at the rate of 100MHz. The complex continuous wave coming from the DDS (implemented using VHDL in the same FPGA) at the rate 100MHz forms an input to this model. Then the process of multiplication, subtractions etc follow. The output of the design is scaled and interpreted at each stage keeping in mind the number of bits and data format requirements. The filter used to filter the output is designed using FDA tool of FPGA. The specifications of the filter are Fc1= 36.3 MHz, Fc2= 43.7 MHz, attenuation = 80 dB, band pass FIR filter, 51 taps. The Xilinx System Generator (XSG) design tool provides logic synthesis as well as bit and cycle-true simulation capabilities within the Simulink environment. These models have been evaluated both for logic and timing in the simulation environment as well as on hardware. The responses obtained were in agreement with the required specifications. The output of FPGA is shown below.

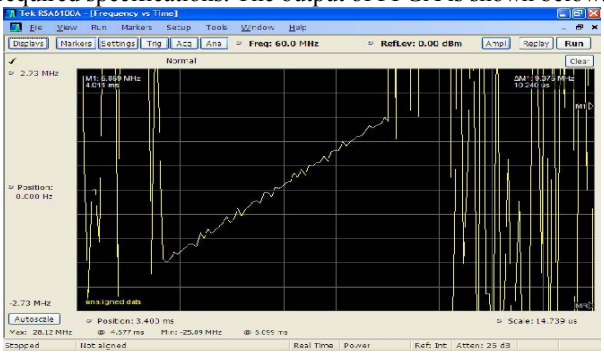

Fig7: Frequency Vs Time Plot of FPGA Output

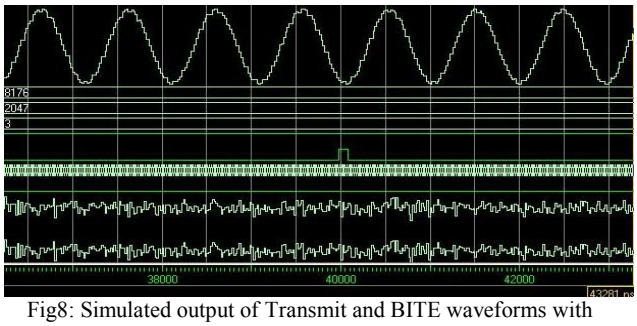

Fig8: Simulated output of Transmit and BITE waveforms with added noise and delay levels.

IV. APPLICATIONS

It can be used in many ways as follows but not limited to

A. Air Traffic Control
B. Ship Safety
C. Military
D. Law Enforcement
E. Military
F. Remote Sensing
G. Space
H. Law Enforcement

CONCLUSION

Thus, the paper explains the digital methodology behind the realization of waveform generation. These digital methods facilitate the Radar signal generator with high degree of flexibility. In the digital waveform generation function based on the pulse characteristics and modulation schemes, the respective waveform code sample may vary. These samples will be stored in the respective memory modules. But this unique design model can be used for the generation of different radar waveforms for different radar systems. The utilization of the customized cores in the design models delivers high level of performance and area efficiency. Thus it resulted in an efficient implementation of the hardware using less percentage of FPGA resources. In addition, digital implementation is advantageous because the system becomes highly flexible, simple and reliable.

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