An Alternate Approach to DPWM Generation for Power Converters using RL Gates

A.D.Senthil Kumar, T.S.Anandhi, S.P.Natarajan

***Abstract*— Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power electronic devices. In this paper FPGA based Digital PWM (DPWM) is developed for power converters in low power applications using Verilog HDL coding and simulated using Modelsim. The advancement in VLSI designs helps particularly portable device technologies by increasing high computation requirements, leading to the design of faster, smaller and more complex electronic systems. Also the use of RL gates reduces the transient delay, improving the switching frequency. High switching frequency optimizes the size of power converters. The implemented digital PWM generator using an FPGA utilizes less memory usage and provides flexible PWM patterns. The simulated result shows an alternative approach to the digital PWM generation by using RL Gates which achieves less consumption of power and area. The resolution and gain of the PWM remain constant regardless of the module clock frequency and PWM output frequency.**

***Index Terms*— FPGA, DPWM, Reversible Gates, Verilog HDL**

I. INTRODUCTION

Digital pulse-width modulators (DPWMs) have become a basic building block in digital control architectures of any power converter [1]–[7]. The DPWM frequency is mainly determined by the power converter operating conditions, whereas the DPWM resolution determines the accuracy in the output voltage/current control[2]. As a consequence, the DPWM resolution has a direct impact in the power converter performance. DPWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

For the control applications of DC-DC buck converters the PWM signals were used to convert unregulated DC voltage to regulated DC voltage at the output[3]. PWM inverters controls the speed of the motor by varying frequency and magnitude of the voltage and current applied to it.

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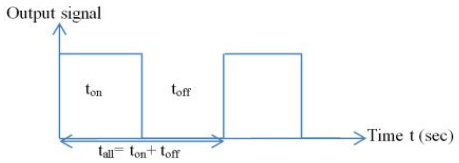

Figure1: PWM Signal

The main advantage of PWM is that power loss is very low in the switching devices. Many digital circuits can generate PWM signals [1]. In this article RL gates are used to generate carrier based PWM in the digital domain using VHDL.

II. REVERSIBLE LOGIC GATES

A reversible logic[8] gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. RL gates have one to one mapping with their input and the output data , zero loss of information [9] ,less power dissipation and latency in the manipulation of any logical operation. They provide the output data ,the input data and the garbage values and hence effective in implementing the Boolean expressions. They also produce unique output data for the unique input data. For determining the complexity and performance of RL gate circuit the following parameters have to be considered

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at
- either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs/ garbage outputs which are essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

Goals of reversible logic

1. Minimize the garbage
2. Minimize the width of the circuit
3. Minimize the total number of gates
4. Minimize the delay

A. BME GATE

A 4*4 RL gate named BME gate is proposed. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The outputs are defined as
P=A,
Q=AB⊕C,
R=AD⊕C and
S=$\bar{A}$B⊕C⊕D.

The block diagram of BME gate is shown in Figure 2.

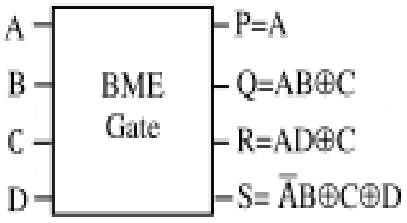

Figure 2: Block diagram of a new reversible BME gate

B.PERES GATE

In 3*3 Peres gate [15],the input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined as
P = A,
Q = A⊕B and
R=AB⊕C.
Quantum cost of a Peres gate is 4. Figure 3 shows a 3*3 Peres gate.

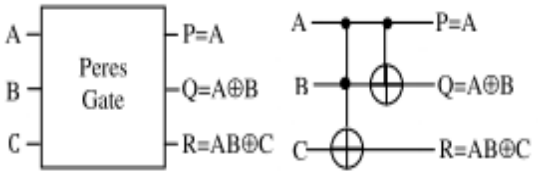

Figure 3: Peres gates

C. Design of Reversible RS Flip-Flop

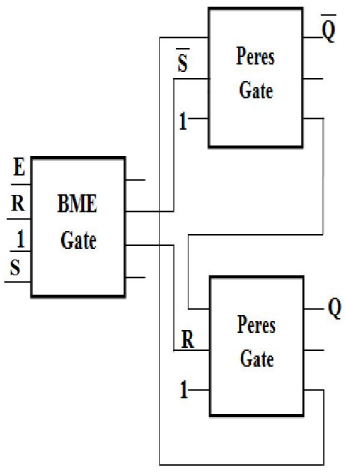

Figure 4 Architecture of reversible RS Flip-Flop

The RS Flip-Flop is mapped with one BME and two Peres gate. The BME gate needs E, S, 1 and R inputs respectively in 1st, 2nd, 3rd and 4th input. The output $\overline{E.S}$ and $\overline{E.R}$ are realized by one BME in the 2nd and 3rd outputs. Now, the 2nd output of $\overline{E.S}$ that is $\overline{S}$ can be used as 2nd input of one Peres gate. The 3rd output of $\overline{E.R}$ that is $\overline{R}$ can be used as 2nd input of another Peres gate. Thus, our design needs only 3 reversible logic gates with 4 garbage outputs to design the RS Flip-Flip. The proposed design of RS Flip-Flip is shown in Figure 4.

III. IMPLEMENTATION OF DPWM

This section discusses the methods of implementing DPWM using RL gates by counter based technique.

A. Counter- based DPWM

This section describes the basic operation of PWM when implemented in the digital domain using a counter. In analog PWM generation, a dc value is continuously compared with a ramp signal. In digital PWM the dc value is compared with the counter value to generate the DPWM signal. A 10 bit duty cycle will be in the range of 0 to 1023. The resolutions of DPWM are finite when compared to the APWM. In other words, DPWM has better output regulation and less or no limit cycle oscillations. Counter based DPWM has modulation delays. These delays occur when there is a change in duty cycle [12, 13,14, 15, 16, 17-20]. Counter based DPWM is implemented using counters as shown in Figure 5.

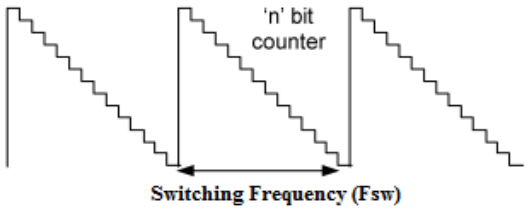

Figure 5:Counter based Carrier Signal

The counter used for the DPWM generation are down counter, up counter, or an up-down counter, which depicts the modulation schemes, the trailing edge modulator ,the leading edge modulator and the dual edge modulator respectively. The input clock frequency (F_{clk}) of the counter is directly proportional to switching frequency (F_{sw}) and number of bits (n). The relationship is expressed as

$$Fclk = Fsw * 2n$$

B. Counter based DPWM using SR Flip Flop

Trailing-edge DPWM block diagram and operational waveform are shown in Figure 6, 7 and 8. The duty cycle and counter are inputs to a comparator. The counter is a up counter. The output of the comparator turns the DPWM pulse on whenever the duty cycle is higher than the counter value. The S-R flip flop sets the DPWM high when the duty cycle is greater than counter value and it resets when the main counter finishes counting to zero. In trailing-edge modulation, the

DPWM is turned on by the clock signal and is turned off by the comparator. In our work, the counter is n-bit up-counter. In this scheme, turning on the DPWM pulse is fixed, and turning off the pulse is done by output of the comparator. Therefore, initially at the starting of switching cycle, the DPWM is turned on, and if the duty cycle value goes below the counter, the comparator outputs a low saturation value (i.e) the DPWM is turned off.

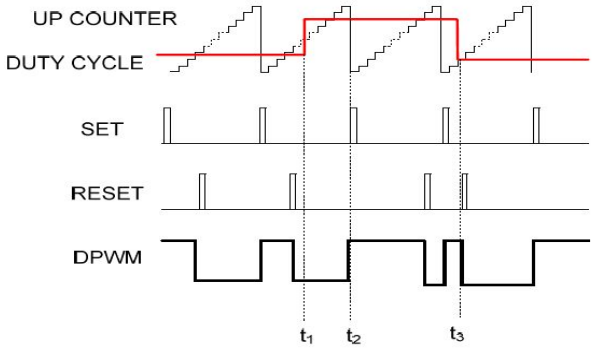

Figure 6: Operation Waveform of Trailing-edge DPWM

The DPWM remains off, even if the duty cycle value is more than the counter value within the same switching cycle, then modulator will not respond to the change it maintains the previous output until the next switching cycle as shown in Figure 6 . Therefore this causes a turn on delay [2, 14, 16, 20].

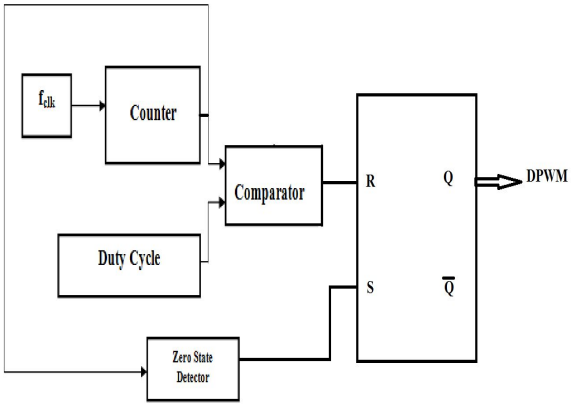

Figure 7: Block diagram of Trailing-edge DPWM using RS Flip Flop

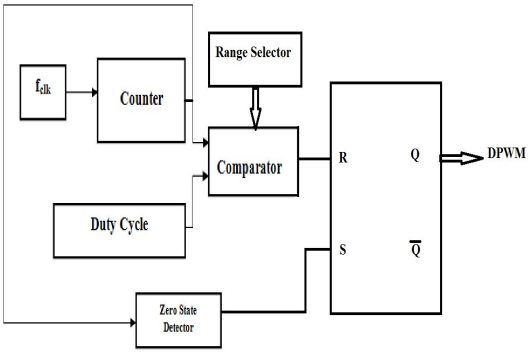

Figure 8: Block diagram of Trailing-edge DPWM Range Selector

The comparator value can be predefined to any value by using Range Selector as shown in Fig.8 in order to achieve the desired frequency ranges from 1MHz to 100 MHz. The comparator output triggers SR flip-flop, which turns the DPWM when the duty cycle is higher than the counter value. DPWM will be turned off only at the end of switching cycle.

C. Counter based DPWM Using RL gates

Block diagram of trailing-edge DPWM using RL gates are shown in Figure 9 and 10. The DPWM sets to high when the duty cycle is greater than counter value and it resets when the main counter finishes counting to zero.

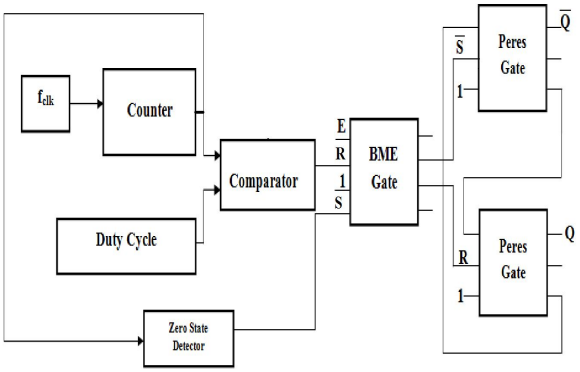

Figure 9: Block diagram of Trailing-edge DPWM using RL Gates

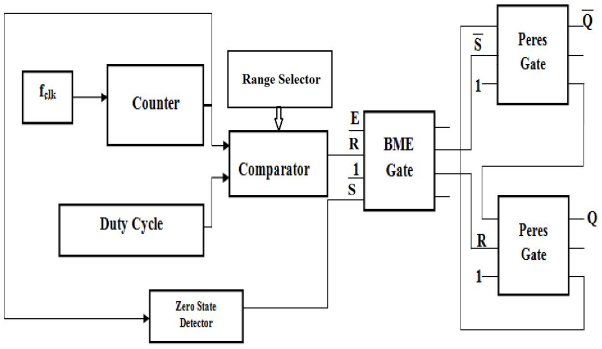

Figure 10: Block diagram of Trailing-edge DPWM using RL Gates with Range Selector

As discussed the comparator can set to predefined value by specifying the range selector as shown in Fig.10 so that the counter counts and sets to high and it resets when the main counter matched with comparator value(Range Selector) in order to achieve the desired frequency which can be ranges from 1MHz to 100 .

IV. EXPERIMENTAL RESULTS

The proposed architecture operation was simulated and synthesized using Modelsim 6.3g and Xilinx ISE 14.2, which contains the Xilinx Spartan-3E FPGA and the device utilization results of the implementation for this device are shown in Synthesis result Table1. The on-board clock running at 50 MHz was used and the resulting PWM frequency with an 24-bit data input was 2.5MHz. The Simulation waveforms

of the PWM output are shown in Fig.11 and Fig.12, respectively..

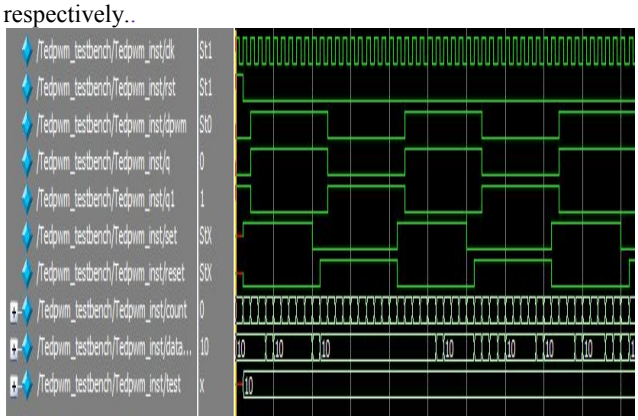

Figure 11: Simulation waveform of trailing-edge DPWM using RS Flip Flop

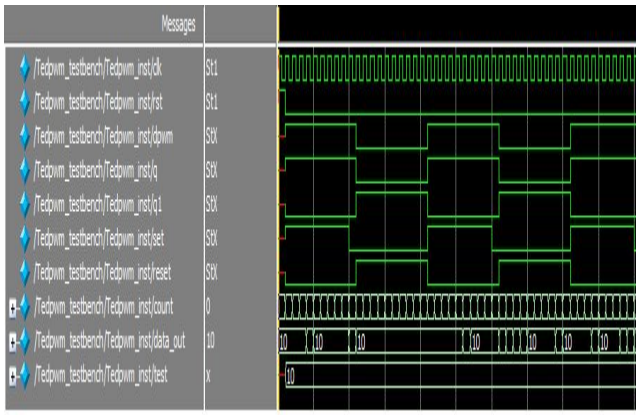

Figure 12: Simulation waveform of trailing-edge DPWM using RL Flip Flop

Fig.11 and 12 shows that the output at Q which produces DWPM is having the duty cycle which based on the comparator. The PWM duty cycle can be varied by changing the data width of Range Selector. In Fig.12 the DPWM produced at Q is based on the Peres Gate.

A. Calculation for Frequency

A Verilog HDL coding was developed, for synthesizing the architecture presented in the previous section, using the Xilinx software 14.1. The Synthesis used device manufactured by Xilinx, such as the FPGAs XC3S500E, SPARTAN-3E with 50MHz Crystal Oscillator can produce variable frequency with the below formula.

$$\text{Desired Switching Frequency} = \frac{\text{Input Frequency*}}{\text{Range**}}$$

$$= \frac{50\text{MHz}}{20}$$

$$= 2.5\text{MHz}$$

*FPGA Oscillator frequency

**Data width specified in design

The resulting maximum clock frequencies, can be achieved by changing the FPGA Boards with different oscillators (frequencies).

B. Synthesis Result

Logic Utilization	DPWM-using SR Flip Flop	DPWM-with RL gates	DPWM using SR Flip flop with Range Selector	DPWM using RL logic with Range Selector
Number of Slices	19	17	76	74
Number of Flip-flops	22	21	69	68
Number of 4 input LUTs	36	33	125	127
Number of bonded IOBs	8	8	3	3
No of GCLKs	1	1	1	1
Max Frequency of Operation(MHz)	196.889	208.986	140.667	148.238

CONCLUSION

In this paper, a Digital PWM generator architecture, using Reversible Logic Gates has been presented. The proposed architecture is based on a special design data width(Range) and can be easily varied in order to achieve the desire frequency. It is observed that RL Gates consumes less area and produce high operating frequency .The resulting PWM frequency depends on the target FPGA device, speed grade and oscillator frequency. The selection of the target device depends on the system cost and resolution requirements.

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