A Novel Design of DC Voltage Controller and Asymmetric Twin Converter Topology based D-STATCOM used for Induction Drive Application

Gamasu.Ramesh, G.Kaladhar, S.V.D Anil Kumar

***Abstract*— Power Electronics (PE) converter technology is a very efficient alternative for medium-voltage and high-power applications and also for other applications where high-quality voltages and currents are required. The main concern of consumers is the quality and reliability of power supplies at various load centers where they are located at .Even though the power generation in most well developed countries is fairly reliable. The controller can balance individual dc capacitor voltages when H-bridges run with different switching patterns and have parameter variations. It has two advantages: 1) the controller can work well in all operation modes (the capacitive mode, the inductive mode, and the standby mode) and 2) the impact of the individual dc voltage controller on the voltage quality is small. This paper suggests further improvements in this topology. A three-phase cascaded H-bridge inverter his control method uses a discrete-time model of the system to predict the future value of the current for all voltage vectors, and selects the vector which minimizes a cost function. In order to improve the performance, a phase-shifted carrier based pulse width modulation technique is used. A mathematical model of the system is derived, based on which a controller for the scheme is designed. The effectiveness of the scheme is verified through detailed simulation study using Matlab/Simulink.**

***Index Terms*— H-bridge inverter, cascaded inverters, voltage source converter (VSC), Pulse width modulation (PWM), Distributed Static compensator (D-STATCOM)**

I. INTRODUCTION

The Applications to those converters to FACTS technology such as, static synchronous compensator (STATCOM) are a flexible ac transmission system device, which is connected as a shunt to the power system, for generating or absorbing reactive power [5]. A STATCOM works in the capacitive mode if it injects reactive power to the power system. A multipulse converter uses more than one voltage source converter (VSC), with common dc link, operating with nearly fundamental switching frequency, and the output of each module is connected in series through the multipulse transformer[7]-[8]. By adjusting the triggering pulses of different VSCs, specified total harmonic distortion (THD)[2] of the injected current is achieved with reduced switching losses as compared to that of single-VSC-based solution

The distributed static synchronous compensator (D-STATCOM) is a flexible ac transmission system device, which is connected as a shunt to the power system, for generating or absorbing reactive power, improving power factor, neglecting harmonics coming from load. [5]. Multi pulse converter uses more than one voltage source converter (VSC), with common dc link, operating with nearly fundamental switching frequency, and the output of each module is connected in series through the multi pulse transformer. By adjusting the trigger ing pulses of different VSCs, specified total harmonic distortion (THD) of the injected current is achieved with reduced switching losses as compared to that of single-VSC-based solution.

The major drawback of this scheme is the high cost and complex structure of the bulky multi pulse transformer. The major drawback of this scheme is the high cost and complex structure of the bulky multipulse transformer [14]-[15].

Multilevel converter technology is a very efficient alternative for medium-voltage and high-power applications and also for other applications where high-quality voltages and currents are required [1], [2]. The other commonly used multilevel topology, i.e., cascaded converter topology [9]–[13], comprises several single-phase H-bridge/full-bridge converters, with separate dc links. The following are the two associated problems of this topology:

1) The size of the dc-link capacitor required is high because the instantaneous power involved with each module varies a twice the fundamental frequency [14],

2) Regulating voltage across a large number of self supported dc-link capacitors makes the controller design complex.

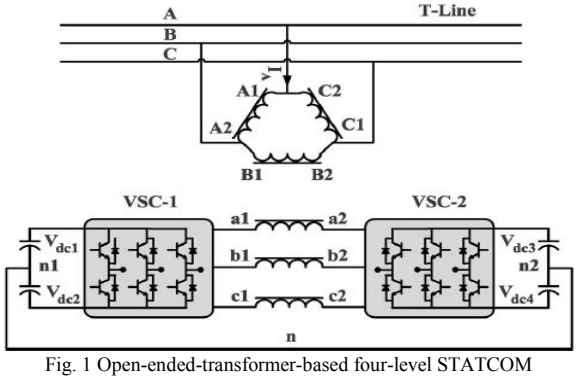

Fig. 1 Open-ended-transformer-based four-level STATCOM

Manuscript received Nov 23, 2015

Gamasu.Ramesh, M.Tech PG Scholar, Department of EEE, St.ANN'S College of Engineering & Technology, Chirala, India

G.Kaladhar, Assistant Professor, Department of EEE, St.ANN'S College of Engineering & Technology, Chirala, India

S.V.D Anil Kumar, Associate Professor & HOD, Department of EEE, St.ANN'S College of Engineering & Technology, Chirala, India

To address some of the aforementioned limitations in multilevel converters, a four-level open-ended transformer-based multilevel converter, shown in Fig. 1, is proposed in [1]. When the multilevel converter is applied to STATCOM, each of the cascaded H-bridge converters should be equipped [9] with a galvanically isolated and floating dc capacitor without any power source or circuit.

This topology uses a reduced number of components (12 controlled switches with [15] anti-parallel diodes) as compared to the diode clamped topology (18 controlled switches with anti-parallel diodes plus 18 diodes) [5]. Moreover, in this case, semiconductor switches are arranged as VSC, which enables easier structural layout and reduced driver circuit complexity.

Therefore, standard VSC power modules include six insulated-gate bipolar transistors (IGBTs) and their driver circuits in one package] can be used instead of discrete components. Moreover, this topology utilizes cascade connection of three-phase VSCs, and hence, the size of the dc-link capacitor is less as compared to that in cascaded H-bridge multilevel converter. Most power-electronics technologies, including control skills, are required to convert the dc into ac power. The open-ended transformer topology has similar component layout with twin converter topology, reported in [2]. In the twin converter topology, the dc-link voltages of both VSCs are maintained equal. Therefore [9], only three-level operation is achieved. However, in the open-ended transformer topology, the dc-link voltage of VSC-2 is regulated to half that of VSC-1. This ensures four-level operation of the circuit [1]. Therefore, low THD is achieved with reduced filter requirements as compared [3] to three-level twin converter topology. The diode-clamped inverter uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors [1]. A matrix of semiconductor switches and diodes allows each phase-leg output to be switched to any of these voltage levels.

A split-capacitor arrangement, used in open-ended transformer- based circuit requires the voltage balancing of the two capacitor banks in each VSC. Therefore, a total of four dc capacitor[20] voltages is to be regulated. This requires a complex controller and generates third-harmonic and dc currents.

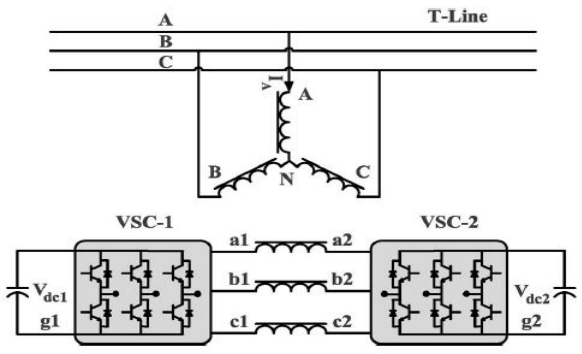

Fig. 2 Asymmetric-twin-converter-topology-based STATCOM

To address this limitation, an asymmetric twin converter topology is proposed in this paper wherein only two dc links are used without split-capacitor arrangement, as shown in Fig. 2. Furthermore, the THD of currents supplied to the grid is reduced by selecting a suitable ratio of dc-link voltages of the two VSCs.

II. Proposed Multilevel Circuit Topology

A. Principle of Operation

The proposed asymmetric-twin-converter-based multilevel topology, comprising two VSCs, is shown in Fig. 2. Low voltage (LV) windings of the transformer are connected differentially between two 2-level VSCs such that the voltage appearing on the LV side is the difference of the output voltages of two VSCs. High-voltage (HV) windings, arranged in a star configuration, are connected to the three-phase grid. Leakage inductances of the transformers act as input filter inductances of the STATCOM. Both VSCs operate with separate dc links to produce two-level individual output. Voltages appearing on the LV windings of the transformer are written in terms of output voltages of VSCs as

$$e_a = e_{a1g1} - e_{a2g2} + e_{g1g2}$$
$$e_b = e_{b1g1} - e_{b2g2} + e_{g1g2}$$
$$e_c = e_{c1g1} - e_{c2g2} + e_{g1g2} \quad (1)$$

Where e_a, e_{a1g1}, e_{a2g2}, and e_{g1g2} are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative dc-link terminals of the two VSCs, respectively. Since both VSCs have separate dc links, the sum of the LV winding phase currents should be zero

$$i_a + i_b + i_c = 0 \quad (2)$$

Furthermore, the sum of instantaneous values of grid voltages is equal to zero

$$v_A + v_B + v_C = 0 \quad (3)$$

The sum of the LV winding voltages is given by

$$e_a + e_b + e_c = \frac{N_{LV}}{N_{HV}}(v_A + v_B + v_C) - r(i_a + i_b + i_c) - L\frac{d(i_a + i_b + i_c)}{dt} \quad (4)$$

Where r and L are the resistance and leakage inductance as measured from the LV side, respectively, and NLV/NHV is the turn's ratio. Substituting (2) and (3) into (4) gives

$$e_a + e_b + e_c = 0 \quad (5)$$

Substituting LV voltages from (1) in (5) results in

$$\begin{aligned} e_{g1g2} &= -\frac{1}{3}(e_{a1g1} - e_{a2g2}) \\ &= -\frac{1}{3}(e_{b1g1} - e_{b2g2}) \\ &= -\frac{1}{3}(e_{c1g1} - e_{c2g2}). \end{aligned} \quad (6)$$

Substituting the value of $eg1g2$ in (1) yields

$$\begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} e_{a1g1} - e_{a2g2} \\ e_{b1g1} - e_{b2g2} \\ e_{c1g1} - e_{c2g2} \end{pmatrix} \quad (7)$$

The relation between LV winding voltages and pole voltages is expressed in (7). Pole voltages depend on the conduction state of the switches in VSC-1 and VSC-2. A total of 26 = 64 different combinations of states of the switches are possible. As discussed in [20], the ratio of dc-link voltages of

VSCs V_{dc1}: V_{dc2} should be equal to 1:0.366 for better performance. Using this, the voltage space vector plot corresponding to unique switching states is shown in Fig. 3. Out of 64 switching states, 49 states produce unique phase voltages, and 25 voltage steps are viable in the LV-side voltage.

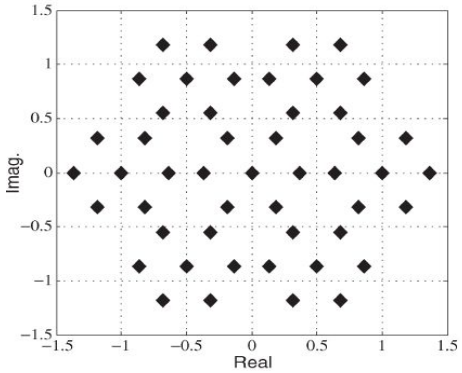

Fig. 3 Space vector diagram of 49 unique states in the proposed topology

The line voltages of the LV side e_{ab}, e_{bc}, and e_{ca} are expressed as pole voltages using (1)

$$e_{ab} = e_a - e_b = e_{a1g1} - e_{a2g2} - e_{b1g1} + e_{b1g2}$$
$$e_{bc} = e_b - e_c = e_{b1g1} - e_{b2g2} - e_{c1g1} + e_{c2g2}$$
$$e_{ca} = e_c - e_a = e_{c1g1} - e_{c2g2} - e_{a1g1} + e_{a2g2} \quad (8)$$

For $v_{dc2} = 0.5v_{dc1}$, depending on the state of switches, voltage waveforms of e_{ab}, e_{bc}, and e_{ca} has seven different steps. This is same as the number of steps obtained in the line voltage of four-level diode clamped multilevel converter. For $v_{dc2} = 0.366v_{dc1}$, nine different steps are observed in the line voltage waveforms, which is the same as that in four-level diode clamped converter with the capacitor voltage ratio v_{dc1} : v_{dc2} : v_{dc3} equal to 0.33:0.66:0.33. This makes the proposed scheme equivalent to a four-level converter.

B. PWM Strategy

LV voltage e_a takes one of the 25 values given by (7), depending on the state of the switches. The switching state is decided by the modulating waveform and the PWM strategy used. Selective harmonic elimination method (SHEM), space vector modulation (SVM), or carrier-based PWM (CB-PWM) techniques are commonly used for high-power applications. SHEM is limited in use because of its slow dynamic response. Realization of SVM for multilevel converter requires an algorithm for the identification of sector. The presence of large number of sectors makes the implementation complex [13].

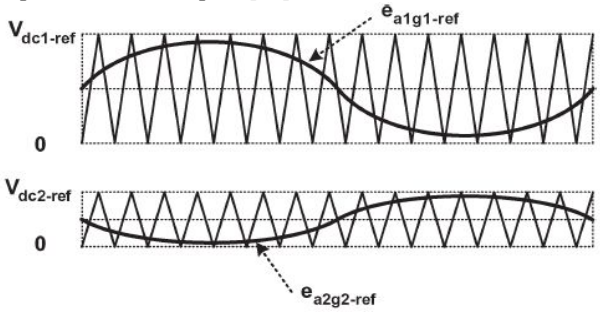

Fig. 4 Comparison of modulating and carrier waveforms for PS CB-PWM

Hence, the use of phase-shifted (PS) CB-PWM is suggested for the proposed topology. This PWM technique expects the controller to generate individual modulating waveforms for each inverter output e_{a1g1}, e_{b1g1}, e_{c1g1}, e_{a2g2}, e_{b2g2}, and e_{c2g2}. Each modulating waveform is compared with a carrier waveform to determine the switching state of the corresponding inverter devices. This is similar to the PS CB-PWM technique used in H-bridge cascaded converters [16], [17]. For two H-bridges per phase, the resultant waveform of ac voltages is the sum of individual converter voltages. Therefore, carrier waveforms are 180◦ PS from each other to cancel the carrier frequency harmonics. However, in the case of asymmetric twin converter topology, the shift in carriers is not required because the resultant waveform is the difference of two ac voltages. Comparison of modulating and carrier signals for phase-a is shown in Fig. 4.The absence of low-order harmonics confirms the operation of PWM technique. Dominant harmonics are present at the sideband of twice the carrier frequency. Although the sidebands of carrier frequency are also present, their magnitude is less than that of twice the carrier frequency.

III. Development of the Equivalent Circuit of the System

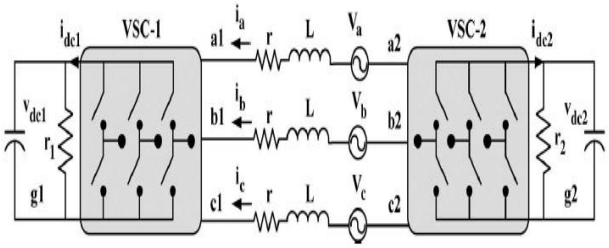

Fig. 5 Equivalent circuit diagram of the proposed STATCOM.

For the purpose of analysis, an equivalent circuit of the proposed STATCOM is derived and is shown in Fig. 5. Transformer is represented by equivalent series combination of inductances, resistances, and voltage sources. To model the losses in two VSCs, two resistances r_1 and r_2 are placed in parallel to the two dc links. The governing equations of the proposed system can be derived as

$$s\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} -\frac{rW_b}{L} & 0 & 0 \\ 0 & -\frac{rW_b}{L} & 0 \\ 0 & 0 & -\frac{rW_b}{L} \end{pmatrix}\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \frac{W_b}{L}\begin{pmatrix} -e_a + V_a \\ -e_b + V_b \\ -e_c + V_c \end{pmatrix} \quad (9)$$

where L is defined as $\omega_b l/z_{base}$. l, ω_b, and $z$base are the leakage inductance, base frequency, and base impedance of STATCOM. All the parameters and variables are expressed in per-unit (p.u.) system. Equation (9) is transformed into dq_0 reference frame, which has been defined in the Appendix. The system variables in the dq_0 frame are expressed as follows:

$$s\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & \omega \\ \omega & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -e_{d1} + e_{d2} + V \\ -e_{q1} + e_{q2} \end{pmatrix} \quad (10)$$

where i_d and i_q are the d- and q-axis components of LV-side currents. e_{d1} and e_{q1} are the voltage components of VSC-1, and e_{d2} and e_{q2} are the voltage components of VSC-2. Equation (10) interrelates the ac parameters of the

STATCOM with those of the grid. The dependence between dc and ac parameters of STATCOM is derived using instantaneous power balance equations. The following equation gives the power balance condition between the ac and dc links of VSC-1:

$$v_{dc1}\, i_{dc1} = \frac{3}{2}\left(e_{d1}\, i_d + e_{q1}\, i_q\right) \quad (11)$$

The current flowing through the dc-link capacitor c_1 is related to the dc-link voltage v_{dc1} as follows:

$$sv_{dc1} = \omega_b C_1 \left(i_{dc1} - \frac{v_{dc1}}{r_1}\right) \quad (12)$$

Where C_1 is defined as $1/(\omega_b c_1 z_{base})$. Substituting i_{dc1} from (11)

$$sv_{dc1} = \omega_b C_1 \left(\frac{3}{2v_{dc1}}\left(e_{d1}\, i_d + e_{q1}\, i_q\right) - \frac{v_{dc1}}{r1}\right) \quad (13)$$

Similarly, the governing equation for VSC-2 is expressed as

$$sv_{dc2} = \omega_b C_2 \left(\frac{3}{2v_{dc2}}\left(e_{d2}\, i_d + e_{q2}\, i_q\right) - \frac{v_{dc2}}{r2}\right) \quad (14)$$

Equations (10), (13), and (14) represent the behavior of the system.

IV. Units Matlab Modeling and Simulation Results

A. Case 1: Proposed Asymmetric Converter Based High Power STATCOM

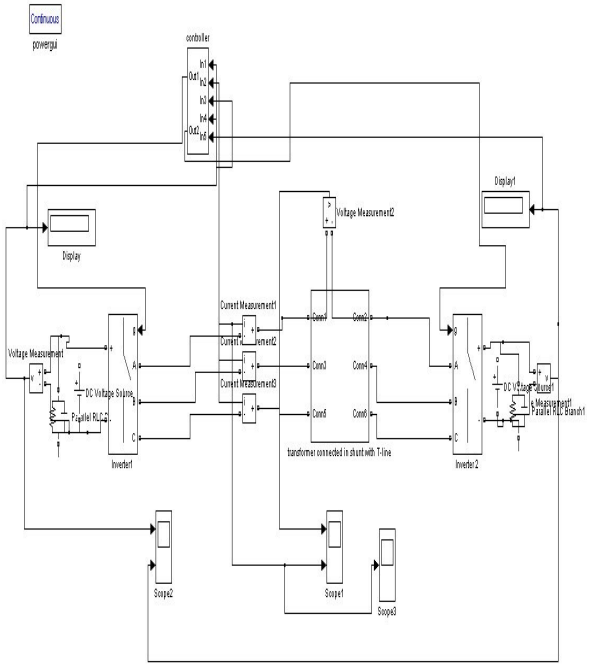

Fig.6 Matlab/Simulink Model of Asymmetric Converter Based High Power STATCOM.

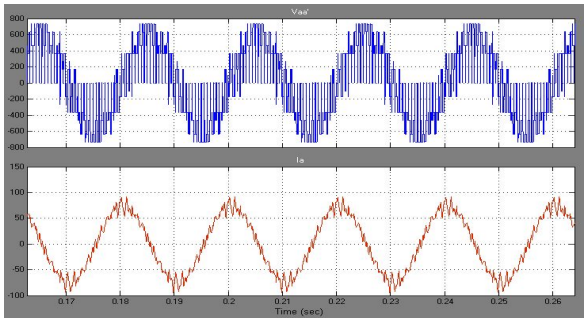

Fig.7 HV-side (grid) phase-a voltage & LV-side phase-a transformer current

As above fig 6 show the Matlab/Simulink Model of Asymmetric Twin Conversion Based High Power STATCOM, Fig.7 shows the HV Side Phase A voltage and LV Side Phase A Transformer Current.

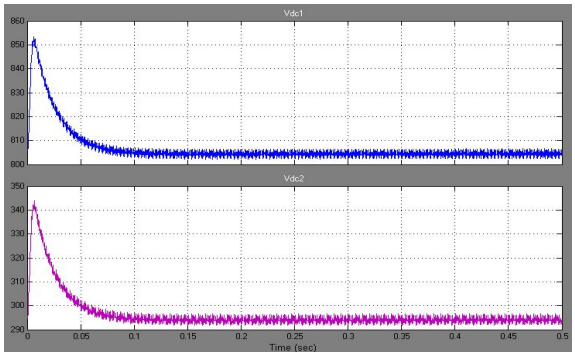

Fig.8 Converter Side Input Voltage

Fig.8 shows the Converter side input voltages, nothing but primary side voltages to support the converter operations with Asymmetric Converter.

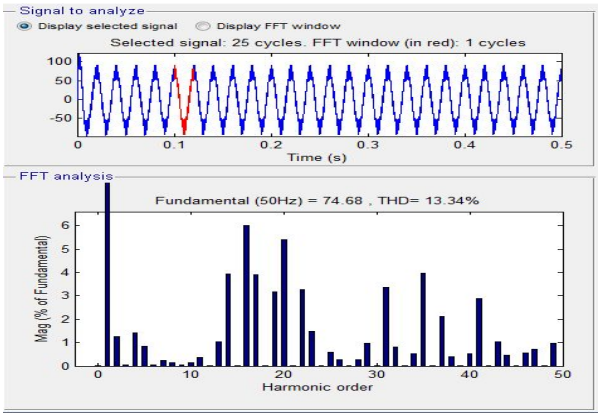

Fig.9 FFT Analysis of LV Side Phase A Current

Fig.9 shows the FFT Analysis of LV Side Phase A Current, we get 13.34%, with Asymmetric Converter.

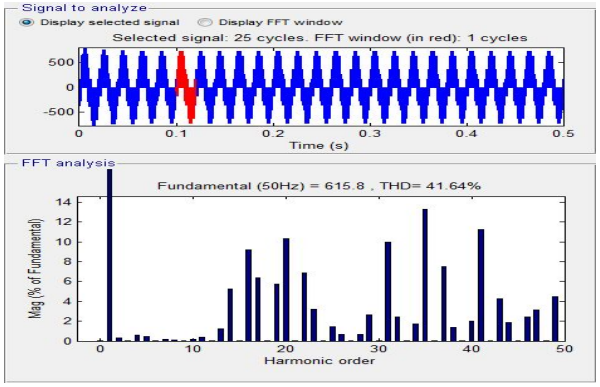

Fig.10 FFT Analysis of LV Side Voltage

Fig.10 shows the FFT Analysis of LV Side Voltage, we get 41.64%, with Asymmetric Converter.

B. Case 2: Proposed Asymmetric Converter Based High Power STATCOM with Reactive Power Control

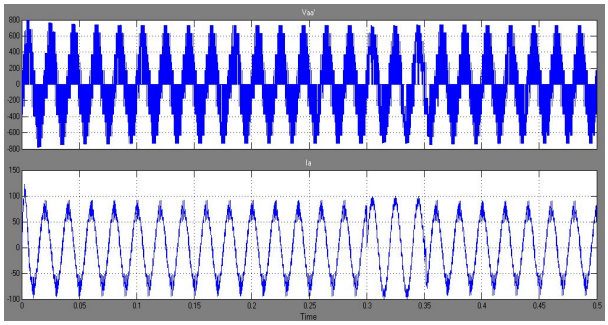

Fig.11 HV-side (grid) phase-a voltage & LV-side phase-a transformer current

Fig.11 shows the HV Side Phase A voltage and LV Side Phase A Transformer Current, with Asymmetric Converter with reactive power control.

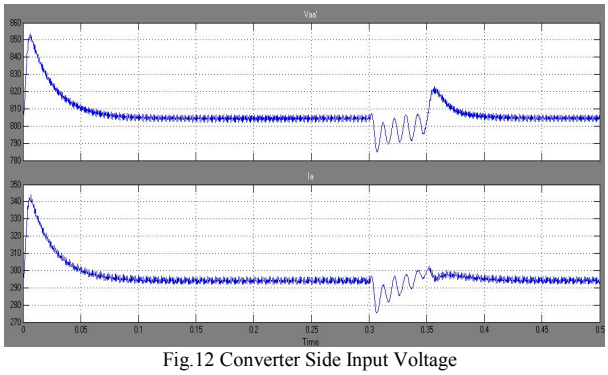

Fig.12 Converter Side Input Voltage

Fig.12 shows the Converter side input voltages, nothing but primary side voltages to support the converter operations with Asymmetric Converter with reactive power control.

C. Case 3: Proposed Asymmetric Converter Based High Power STATCOM Applied to Induction Machine Drive.

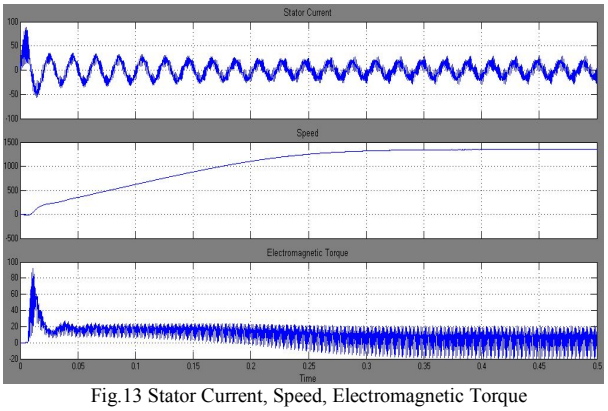

Fig.13 Stator Current, Speed, Electromagnetic Torque

Fig.13 shows the Stator Current, Speed, and Electromagnetic Torque of Proposed Asymmetric Converter Based High Power STATCOM Applied to Induction Machine Drive.

CONCLUSION

Standard VSC power modules (include six insulated-gate bipolar transistors (IGBTs) and their driver circuits in one package) can be used instead of discrete components. Moreover, this topology utilizes cascade connection of three-phase VSCs, and hence, the size of the dc-link capacitor is less as compared to that in cascaded H-bridge multilevel converter. A high-power D-STATCOM based on two 2-level VSCs is proposed with reactive power control and same proposed system applied to induction machine drive to check the performance of the drive, reduced component count, simpler layout of switches, and reduced capacitance requirement are the attractive features of the scheme over the diode clamped and cascaded multilevel converters. In the proposed topology, only two dc voltages have to be controlled. A dc-link voltage controller has been proposed to regulate the dc-link voltages of the two converters by drawing requisite amount of real power from the utility and by differentially distributing them between the two converters. A Matlab/Simulink model of the system is developed to facilitate the design of the proposed converter; we get better response and fast response and better THD values, THD values well within IEEE Standards.

REFERENCES

[1] S. Anand, B. G. Fernandes, and K. Chatterjee, "A new 4-level open-ended transformer based STATCOM for high power applications," in Proc. 36th Annu. IEEE IECON, Nov. 7–10, 2010, pp. 1957–1962.

[2] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAR compensators," Proc. Inst. Elect. Eng. C—Gener., Transm. Distrib., vol. 140, no. 4, Jul.1933,pp. 299–306.

[3] E. M. John, A. Oskoui, and A. Petersson, "Using a STATCOM to retire urban generation," in Proc. IEEE Power Syst. Conf. Expo., Oct. 2004, vol. 2, pp. 693–698.

[4] K.N.V Prasad, G.Ranjith Kumar, T. Vamsee Kiran, G.Satyanarayana., "Comparison of different topologies of cascaded H-Bridge multilevel inverter," Computer Communication and Informatics (ICCCI), 2013 International Conference on , Jan. 2013, pp.1,6, 4-6.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, Aug. 2002, pp. 724–738.
[6] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," IEEE Trans. Ind. Electron., vol. 53, no. 5, Oct. 2006, pp. 1512– 1521.
[7] K.N.V. Prasad, G.Ranjith Kumar, Y.S. Anil Kumar, G. Satyanarayana, "Realization of cascaded H-bridge 5-Level multilevel inverter as Dynamic Voltage Restorer," Computer Communication and Informatics (ICCCI), 2013 International Conference on , Jan. 2013, vol., no., pp.1,6, 4-6.
[8] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, Aug. 2010, pp. 2553–2580.
[9] F. Z. Peng, J. W. McKeever, and D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," IEEE Trans. Ind. Appl., vol. 34, no. 6, Nov./Dec. 1998, pp. 1293–1298.
[10] K. V. Patil, R. M. Mathur, J. Jiang, and S. H. Hosseini, "Distribution system compensation using a new binary multilevel voltage source inverter," IEEE Trans. Power Del., vol. 14, no. 2, , Apr. 1999, pp. 459–464.
[11] C. K. Lee, S. Y. Ron Hui, and H. S. Chung, "A 31-level cascade inverter for power applications," IEEE Trans. Ind. Electron., vol. 49, no. 3, , Jun. 2002, pp. 613–617.
[12] G.Satyanarayana., K.N.V Prasad, G.Ranjith Kumar, K. Lakshmi Ganesh, "Improvement of power quality by using hybrid fuzzy controlled based IPQC at various load conditions," Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on , April 2013, vol., no., pp.1243,1250, pp.10-12.
[13] Y. Fukuta and G. Venkataramanan, "DC bus ripple minimization in cascaded H-bridge multilevel converters under staircase modulation," in Proc. 37th IEEE IAS Annu. Meeting, 1988–1993 vol. 3, pp.12-18.
[14] S. Vazquez, J. I. Leon, J. M. Carrasco, L. G. Franquelo, E. Galvan,
[15] M. Reyes, J. A. Sanchez, and E. Dominguez, "Analysis of the power balance in the cells of a multilevel cascaded H-bridge converter," IEEE Trans. Ind. Electron., vol. 57, no. 7, , Jul. 2010, pp. 2287–2296.
[16] S. Lu, S.Mariethoz, and K. A. Corzine, "Asymmetrical cascade multilevel converters with noninteger or dynamically changing DC voltage ratios: Concepts andmodulation techniques," IEEE Trans. Ind. Electron., vol. 57, no. 7, , Jul. 2010, pp. 2411–2418.
[17] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla, and J. M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single dc source," IEEE Trans. Ind. Electron., vol. 56, no. 7, , Jul. 2009, pp. 2513–2521.
[18] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converterbased STATCOM," IEEE Trans. Ind. Electron., vol. 55, no. 1, , Jan. 2008, pp. 21–29.
[19] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-bridge inverters," IEEE Trans. Ind. Electron., vol. 57, no. 8, , Aug. 2010, pp. 2691–2699.
[20] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, , Aug. 2010, pp. 2633–2642.

Mr. Gamasu. Ramesh received B.Tech Degree in Electrical and Electronics Engineering from JNT University, Kakinada, A.P, India in 2010. Presently, he is M.Tech PG Student Scholar in from Department of Electrical & Electronics Engineering, St.ANN'S College of Engineering & Technology, Cherala, A.P, India. He is member of various Engineering societies like IAENG, IACSIT and, UACEE etc. He attended various workshops and technical seminars at graduation level. He attended and communicated one international conference at SACET, Cherala, India. His areas of interest include FACTS Technology, Deregulation in power systems and Harmonics study in power systems.

Mr.G.Kaladhar received B.Tech. in Electrical and Electronics Engineering from JNT University, Hyderabad in 2003 and M.Tech in Power and Industrial Drives from JNT university, Kakikinada in 2006. Presently Pursuing Ph.D from Department of Electrical Engineering, SV University, Tirupathi, A.P, India. He had been working as Assistant Professor in EEE Department, St.ANN'S College of Engineering & Technology, Cherala, A.P, India from 2006 to till. Mr.G.Kaladhar is an author of 1 journal and attended various workshops and faculty development programs. He is life member of MISTE Society. His Area of research and study interests includes FACTS Technology, Recent Trends in Power Systems.

Mr.S. V. D. Anil Kumar received B.Tech in Electrical and Electronics Engineering from SV University, Tirupathi, India in 2000, M.Tech in Power Electronics from Visveswaraiah Technological University, Belgaum, India in 2005. Presently, he is Head of the department and Associate Professor in the Department of Electrical & Electronics Engineering, St.ANN'S College of Engineering & Technology, Cherala, A.P, India. He has 15 years of Teaching and Industrial, Research Experience and now he is a Ph.D Research Scholar in Electrical Engineering Department, JNT University, Hyderabad, India. Mr.S. V. D. Anil Kumar is an author of more than 15 journal and conference papers.

He attended and conducted various technical workshops and faculty development programs. He is Life member of ISTE, Member in IAENG, IACSI etc. His research and study interests include power quality, Harmonics in Power Systems.