Simulation of a New Quasi Resonant DC Link Inverter to Reduce Switching Losses

J.Pranesh Jonathan, K.Somasekar, J.Rajesh

Abstract— **In this paper a new three phase DC link soft switching inverter is introduced. The auxiliary circuit of the proposed inverter is composed of two switches beside the DC link switch. All switches in the proposed inverter are soft switched. The proposed auxiliary circuit provides zero voltage switching condition for the main inverter switches independent of the link current direction. An analysis of this inverter topology is presented and various operating modes are explained in details. The inverter simulation is performed to validate the analysis.**

***Index Terms*— Soft switching; zero voltage switching; zero current switching; quasi resonant DC link.**

I. INTRODUCTION

Inverters are found in several industrial applications such as uninterruptible power supplies (UPS), motor drives, induction heating, etc. The frequency of hard switching inverters is limited due to: (1) switching losses, (2) severe di/dt or dv/dt which causes Electromagnetic Interference (EMI), and (3) switching stresses (high voltage and current peaks) on the power devices during the turn on and/or turn off transients [1]. By applying soft switching techniques, the switching frequency can be increased [2]-[6].
Soft switching techniques can reduce EMI as well as switching losses and switching stresses.

Therefore, higher switching frequencies can be obtained using soft switching techniques. At high switching frequencies, harmonic filtering is easier and audible noise can be eliminated. In order to provide soft switching condition, a high frequency resonant circuit is added to the conventional hard switching inverter. The resonant circuit can be composed of passive elements, diodes and switches. Depending on the position of the auxiliary circuit, soft switching inverters are defined. In DC link inverters, the auxiliary circuit is between the DC source and inverter main switches. When the state of inverter switches should change, the auxiliary circuit is turned on and the inverter DC link voltage is reduces to zero and thus, the state of inverter switches can be changed under zero voltage switching (ZVS) condition.

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The resonant DC link (RDCL) concept was first proposed in [7]. This inverter had many drawbacks such as high voltage stress of the switches, high DC link voltage ripple and it could only operate with discrete pulse modulation (DPM) control that is hard to achieve while resulting in sub-harmonics. Furthermore the inductor power losses were considerable as the inductor always conducts. To overcome RDCL drawbacks, actively clamped resonant DC link (ACRDC) technique was introduced in [8]. The ACRDL technique reduces the switch voltage stress to 1.2-1.4 times the source voltage. However, it is difficult to control current balance of clamp capacitor.
In [9] a new ACRDC is introduced. The clamping circuit has a small DC source which itself is a problem.
Another problem is that the energy of DC link capacitor is not recovered and is dissipated. In order to provide ZVS condition for inverter switches, several quasi resonant schemes are introduced [10]-[15]. The circuit proposed in [10], consists of four switches which three of them are turned off under hard switching condition. The topology introduced in [11] has three switches but two switches are turned off under hard switching condition. This paper introduces a new quasi resonant DC link inverter which provides ZVS condition for the main inverter switches at transition instants. The auxiliary circuit has three switches which all of them are soft switched. The proposed inverter is analyzed and the operating modes are discussed. Finally the inverter is simulated using PSPICE software to justify the analysis.

II. CIRCUIT DESCRIPTION AND OPERATION

The proposed inverter is shown in Fig. 1. This inverter is composed of a conventional three phase inverter and the auxiliary circuit. The auxiliary circuit consists of three auxiliary switches, two diodes, two resonant capacitors, one resonant inductor and two coupled inductors

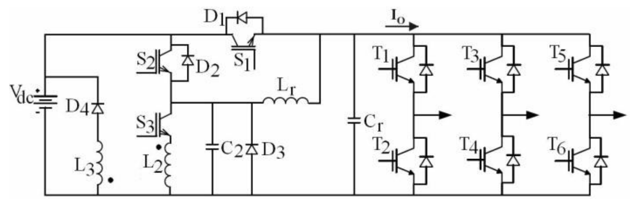

Figure 1. Power circuit configuration of the proposed inverter

Since the inductors of the auxiliary circuit are much smaller than the load inductors, the inverter switches and three phase load can be replaced by a constant current load during one switching cycle. The equivalent circuit of the inverter is shown in Fig. 2. The inverter has 12 operating modes in a switching cycle. The corresponding waveforms of the auxiliary switches, gate signals, capacitors voltages, inductors currents and the currents of diodes are shown in Fig. 3. The equivalent circuit of each operating mode is illustrated in Fig. 4.

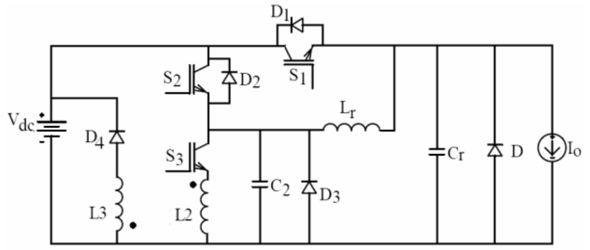

Figure 2. Equivalent circuit of the proposed inverter

Before the first mode it is assumed that current flows from the dc power supply to the load through switch S1. The voltage across capacitors Cr and C2 is equal to the supply voltage Vdc and switches S2 and S3 are off.

Mode 1 (t0 to t1): When the inverter main switches require changing conduction mode, DC link voltage must be reduced to zero. Thus, in this mode, switch S1 is turned offunder ZVS (due to Cr) and switch S3 is turned on under ZCS (due to L2) at the same time. Therefore, Cr, C2, Lr and L2resonate. Since capacitor C2 is small, VC2 decreases to zero very fast, thus the slow resonance between Cr and Lr is omitted
in this mode. Energy of C2 is transferred to the inductor L2 andiL2 increases. During this mode VCr and iLr are assumed almost constant.
With initial conditions VC2 (t0) □ Vdc, iL2 (t0) □ 0 the equations can be written as following:

$$i_{L2}(t) = \frac{V_{dc}}{z_0}\sin(\omega_0 t) \tag{1}$$

$$V_{C2}(t) = V_{dc}\cos(\omega_0 t) \tag{2}$$

$$\Delta t_1 = t_1 - t_0 = \frac{\pi}{2\omega_0} \tag{3}$$

$$z_0 = \sqrt{\frac{L_2}{C_2}},\ \omega_0 = \frac{1}{\sqrt{L_2 C_2}} \tag{4}$$

Mode 2 (t1 to t2): This mode begins when VC2 reaches zero and diode D3 starts conducting. Due to the resonance between capacitor Cr and inductor Lr, VCr decreases and iLr increases. With initial condition VCr (t1) □ Vdc , iLr (t1) t0 , the important equations of this mode are:

$$i_{Lr}(t) = I_o - I_o\cos(\omega_1 t) - \frac{V_{dc}}{z_1}\sin(\omega_1 t) \tag{5}$$

$$V_{Cr}(t) = +V_{dc}\cos(\omega_1 t) - I_o z_1 \sin(\omega_1 t) \tag{6}$$

$$i_{L2}(t) = \frac{V_{dc}}{z_0} \tag{7}$$

$$z_1 = \sqrt{\frac{L_r}{C_r}},\ \omega_1 = \frac{1}{\sqrt{L_r C_r}} \tag{8}$$

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_1}\tan^{-1}\left(\frac{V_{dc}}{I_o z_1}\right)$$

Mode 3 (t2 to t3): In this mode, DC link voltage is zero. Diode D is turned on and Io flows through it. During this mode, the inverter switches can be either turned on or turned Off under ZVS condition.

$$i_{Lr}(t) = i_{Lr}(t_2) \tag{10}$$

$$i_{L2}(t) = i_{L2}(t_2) \tag{11}$$

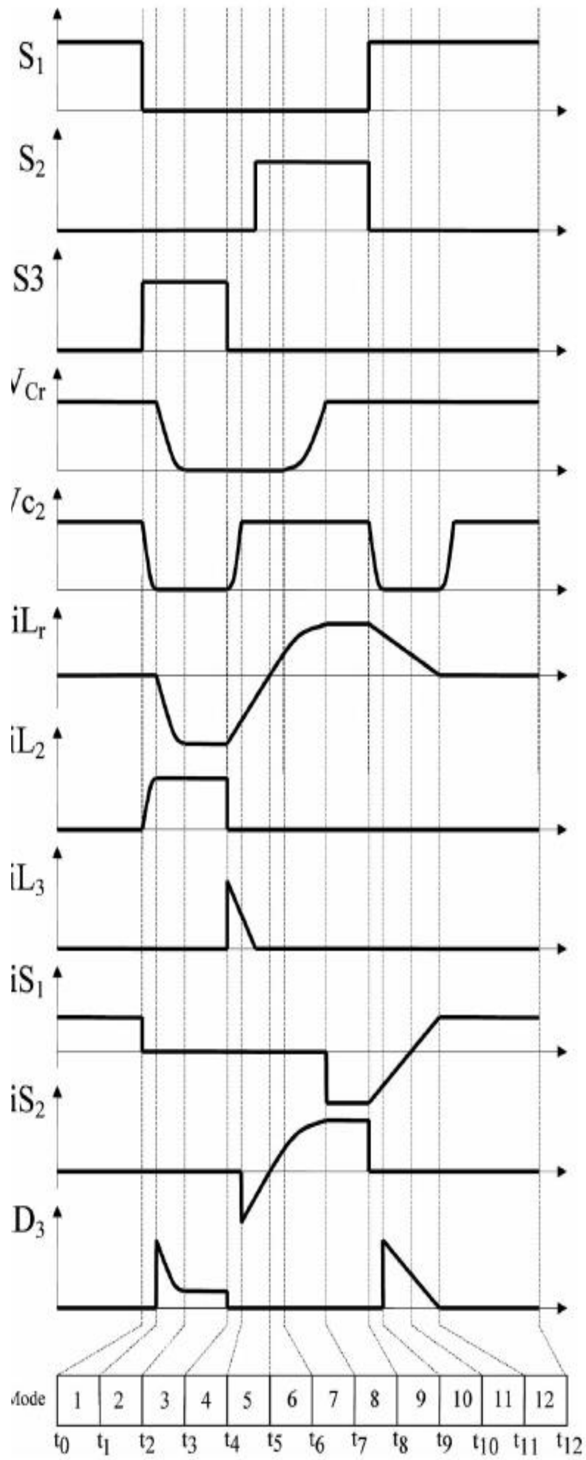

Figure 3. Key waveforms of the inverter equivalent citcuit

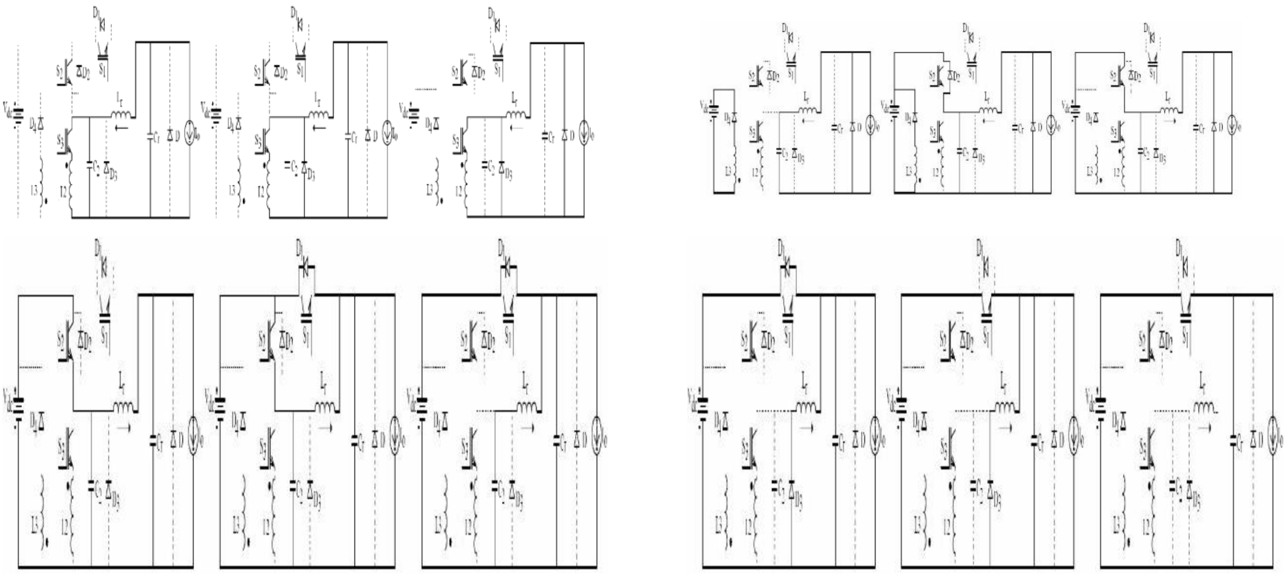

Figure 4. Equivalent circuits during various modes of operation

Mode 4 (t3 to t4): In this mode, S3 is turned off. Thus, D4 is turned on and the energy of L2 is transferred to the inductor L3. By considering L3 turns much higher than L2 turns, the voltage across L2 would be negligible and S3 turn off is under almost ZVS condition due to C2. Important equation of this mode is:

$$i_{L3}(t)=i_{L2}(t_2)\sqrt{\frac{L_2}{L_3}}-\frac{V_{dc}}{L_3}t \qquad (12)$$

Also, inductor Lr and capacitor C2 resonate and VC2increases to Vdc. With initial condition VC2 (t3) the following equations are obtained:

$$i_{Lr}(t)=i_{Lr}(t_3)\cos(\omega_2 t) \qquad (13)$$

$$V_{C2}(t)=-i_{Lr}(t_3)z_2\sin(\omega_2 t) \qquad (14)$$

$$z_2=\sqrt{\frac{L_r}{C_2}},\ \omega_2=\frac{1}{\sqrt{L_r C_2}} \qquad (15)$$

$$\Delta t_4=t_4-t_3=\frac{1}{\omega_2}\sin^{-1}\left(-\frac{V_{dc}}{z_2 i_{Lr}(t_3)}\right) \qquad (16)$$

Mode 5 (t4 to t5): When VC2 reaches Vdc, diode D2turns on. In this mode, iLr is shifted to diode D2 and the energy stored in inductor Lr is recovered and iLr decreases linearly to zero. In this mode, switch S2 can be turned on under zero voltage-zero current (ZVZCS) condition.

With initial condition VC2 (t4) Vdc the following equations are obtained:

$$i_{Lr}(t)=i_{Lr}(t_4)-\frac{V_{dc}}{L_r}t \qquad (17)$$

$$\Delta t_5=t_5-t_4=\frac{L_r i_{Lr}(t_4)}{V_{dc}} \qquad (18)$$

Mode 6 (t5 to t6): In this mode, iLr increases linearly in the opposite direction while the current through diode D decreases. The load current is diverted from freewheeling diode D to switch S2 and inductor Lr but VCr is still equal to zero.

With initial condition $i_{Lr}(t_5)=0$

$$i_{Lr}(t)=\frac{V_{dc}}{L_r}t \qquad (19)$$

$$\Delta t_6=t_6-t_5=\frac{L_r I_o}{V_{dc}} \qquad (20)$$

Mode 7 (t6 to □ t7): This mode starts when Lr current reaches Io and diode D turns off. Thus, Cr is charged in a resonance with inductor Lr. Current iLr is equal to the sum of the charging current of capacitor Cr and the link current Io. The DC link voltage increases from zero to the source voltage Vdc. With initial condition VCr (t6) □ 0 , iLr (t6) □ Io the equations can be written as following:

$$i_{Lr}(t)=\frac{V_{dc}}{z_1}\sin(\omega_1 t)+I_o \qquad (21)$$

$$V_{Cr}(t)=-V_{dc}\cos(\omega_1 t)+V_{dc} \qquad (22)$$

$$\Delta t_7=t_7-t_6=\frac{\pi}{2\omega_1} \qquad (23)$$

Mode 8 (t7 □ t □ t8): Further increase in the DC linkvoltage due to the resonance between inductor Lr and capacitorCr causes the anti-parallel diode of switch S1 to be forward biased and VCr is clamped at Vdc. Since current Lr is more thanthe load current, the extra current flows through diode D1.Thus

$$i_{Lr}(t)=I_o+\frac{V_{dc}}{z_1} \qquad (24)$$

Mode 9 (t8 to t9): In this mode, switch S2 is turned off under ZVS (due to capacitor C2). Inductor Lr and capacitor C2resonate and the energy of C2 is transferred to Lr. At the end of this mode, VC2 is zero. In this mode, switch S1 can be turned on under ZVZCS condition. With initial condition VCr (t8) □ Vdc the following equations are obtained.

$$i_{Lr}(t) = i_{Lr}(t_8)\cos(\omega_2 t) \qquad (25)$$

$$V_{Cr}(t) = -i_{Lr}(t_8) z_2 \sin(\omega_2 t) + V_{dc} \qquad (26)$$

$$\Delta t_9 = t_9 - t_8 = \frac{1}{\omega_2}\sin^{-1}\frac{V_{dc}}{i_{Lr}(t_8) z_2} \qquad (27)$$

Mode 10 (t9 to t10): When VC2 reaches zero, the resonance between inductor Lr and capacitor C2 stops. DiodeD3 is turned on and iLr flows through diode D3.With initial condition VCr (t9) the following equations are obtained:

$$i_{Lr}(t) = i(t_9) - \frac{V_{dc}}{L_r} t \qquad (28)$$

$$\Delta t_{10} = t_{10} - t_9 = \frac{L_r (i(t_9) - I_o)}{V_{dc}} \qquad (29)$$

Mode 11 (t10 to t11): This mode starts when diode D1turns off and at the same time, switch S1 starts conducting. The load current is sum of the inductor current and current through S1. When all the energy stored in the inductor Lr is recovered, this mode ends. With initial condition iLr (t10) □ Io the equations of this mode are:

$$i_{Lr}(t) = I_o - \frac{V_{dc}}{L_r} t \qquad (30)$$

$$\Delta t_{10} = t_{11} - t_{10} = \frac{L_r I_o}{V_{dc}} \qquad (31)$$

Mode 12 (t11 to t12): In this mode the inverter operation is the same as a conventional inverter. Current flows from DC source through switch S1 to the load and VCr and VC2 are equal to Vdc.

III. CONTROL SCHEME

The main inverter switches are controlled like a Conventional PWM inverter. Three 120 degrees shifted sine waves are compared with a saw tooth waveform and PWM signals are generated as shown in Fig. 5. When a change in main inverter switches is needed, switch S1 should be turned off and switch S3 should be turned on. Thus, after a delay, the DC link voltage becomes zero and the inverter main switches can change state under zero voltage condition. This delay can be calculated from equations (3) and (9). When inverter main switches change their states, the DC link voltage should return back to Vdc and thus switch S3 is turned off and switch S2 is turned on. After a delay, capacitor Cr is charged. This delay can be obtained by equations (18), (20) and (23). When VCr is equal to the supply voltage Vdc, switch S2 is turned off and switch S1is turned on and the operation principle is the same as a conventional inverter. The schematic of the control circuit is shown in Fig. 6.

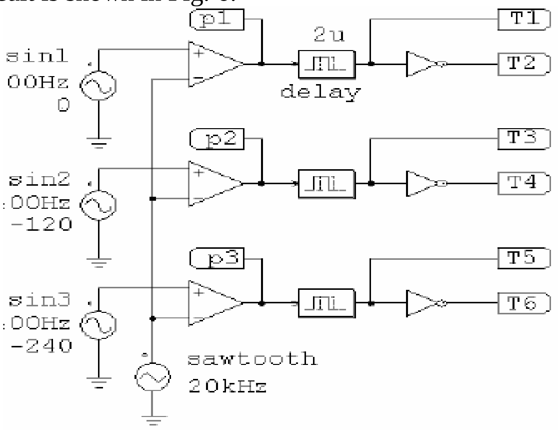

Figure 5. PWM generating circuit

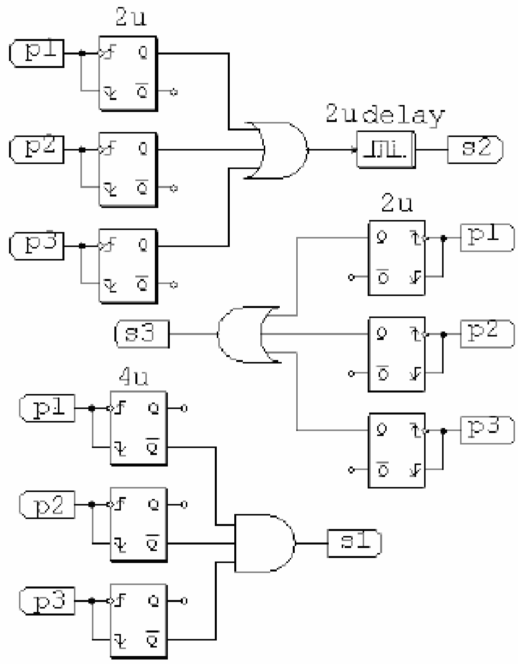

Figure 6. Control circuit diagram

IV. SIMULATION RESULTS

The proposed quasi resonant DC link inverter is simulated by pspice software to demonstrate the features and appropriateness of theoretical analysis. The simulation is performed at input voltage source Vdc of 200V, Cr=20nF, C2=.6nF, Lr=15μH, L2=3μH and L3=300μH.

Fig. 7 shows the current and voltage operating waveforms of switch S1. The waveforms confirm ZVZCS at turn on and ZVS at turn off for switch S1. Fig. 8 illustrates the current and voltage operating waveforms of switch S2. It shows that switch S2 is turned on under ZVZCS condition and is turned off under ZVS condition. Operating waveforms of switch S3 are shown in Fig. 9. Switch S3 is turned on under ZCS and turned off under ZVS.

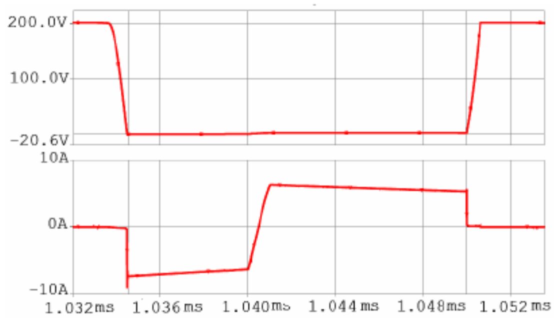

Figure 7. Top: switch S1 voltage, bottom: switch S1 current

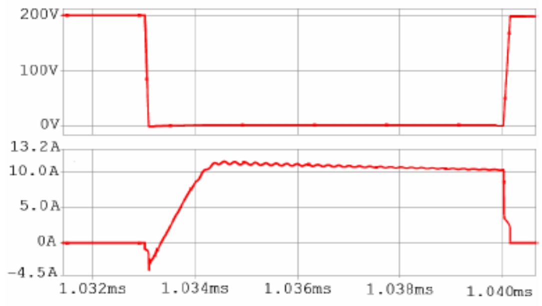

Figure 8. Top: switch S_2 voltage, bottom: switch S_2 current

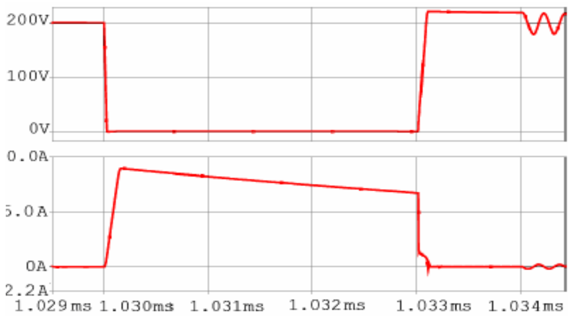

Figure 9. Top: switch S_3 voltage, bottom: switch S_3 current

Current and voltage waveforms of one of the inverter main switches are shown in Fig. 10. The waveforms of three phase output currents at 400 Hz are shown in Fig. 11. Figure 10 and 11 are obtained using PSIM software. Once the resonance frequency for discharging the link capacitor is selected much higher than inverter switching frequency, the auxiliary circuit does not have any important effect on the operation of the PWM inverter. In other words, since the duration of auxiliary circuit operation in each switching cycle is very small, its effect on the output waveforms will be negligible.

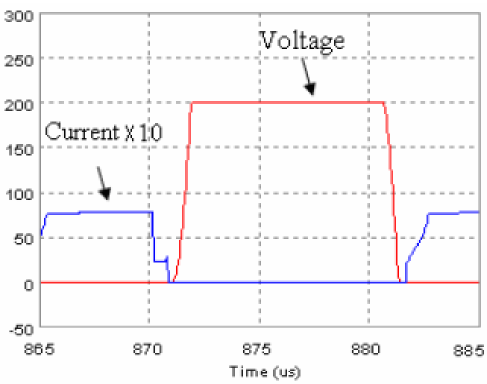

Figure 10. Current and voltage waveforms of one of the inverter main switches

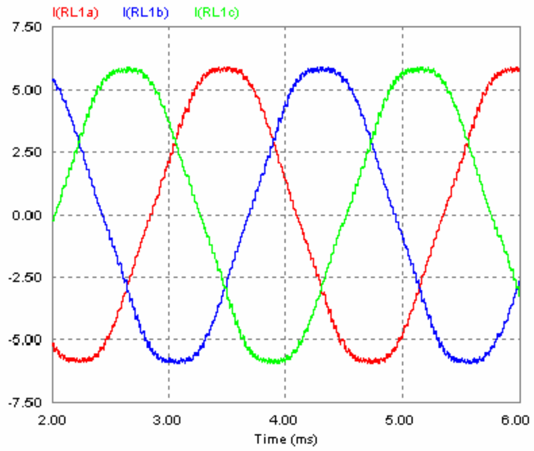

Figure 11. Three phase output currents

CONCLUSION

In this paper, a new quasi resonant DC link inverter is proposed. The auxiliary circuit consists of three auxiliary switches. All switches in the proposed inverter turn on and off under ZVS or ZCS condition. The proposed inverter is analyzed and all operating modes are discussed. Validity of theoretical analysis is confirmed using simulation results.

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