Cascaded Multilevel Inverters Design and Its Furtherance

R.Karthika, T.jothi, M.Preetha, M.Yuvallela

Abstract— **The multilevel inverter collectively converters the several levels of dc voltage to a desired ac voltage. Multilevel inverter incorporates various pulse-width modulation Strategies.The unique structure of multilevel inverters allows them to reach nearer to sinusoidal i.e. with low harmonics. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases. The increase of voltage levels with low ratings of individual devices can increase the power rating. To produce a high-power, high-voltage inverter with multilevel structure is easy, as the device voltage stresses are controlled in the structure. The use of a high-voltage inverter makes possible. For the direct connection to the high-voltage distribution system, eliminating the distribution Transformers. An inverter can produce a controlled reactive current and operates as a Static VAR Compensation in steady state operation. The most common applications of multilevel inverters include Reactive power compensation, Back-to-Back inter-tie &Variable speed drives. The multilevel inverters are classified as Diode clamped, flying capacitor & cascaded multilevel inverters. These topologies of multilevel inverters are discussed and new topology, proposed from cascaded multilevel inverter has been introduced. The Simulated results have been obtained for Cascaded multilevel inverter &Proposed modified cascaded multilevel inverter using continuous and SPWM techniques**

Index Terms—**About four key words or phrases in alphabetical order, separated by commas.**

I. INTRODUCTION

In general, increasing the switching frequency in voltage source inverters (VSI) leads to the better output voltage / current waveforms. Harmonic reduction in controlling a VSI with variable amplitude and frequency of the output voltage is of importance and thus the conventional inverters which are referred to as two-level inverters have required increased switching frequency along with various PWM switching strategies. In the case of high power high voltage applications, however, the two-level inverters have some limitations to operate at high frequency mainly due to switching losses and constriction of device rating itself. Moreover, the semiconductor switching devices should be used in such a manner as problematic series / parallel combinations to obtain capability of handling high power. Nowadays the use of multilevel approach is believed to be promising alternative in such a very high power conversion processing system. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation.

Multi-level inverters are the modification of basic bridge inverters.They are normally connected in series to form stacks of level In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

It should have less switching devices as far as possible.

It should be capable of enduring very high input voltage such as HVDC transmission for high powerApplications.

Each switching device should have lower switching frequency owing to multilevel approach.

II. CASCADED MULTILEVEL INVERTER

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. There are different types of multi level circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected[2].Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels

The modularity of this structure allows easier maintenance and provides a very convenient way to add redundancy into the system. The multilevel inverter using cascaded-inverter with separate DC sources synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This

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configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase 3- level configuration of such an inverter is shown in Fig 2.1

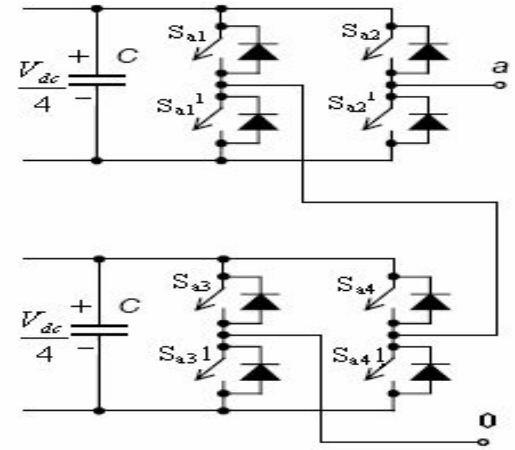


Fig 2.1 Single Leg Five Level Cascaded Multilevel Inverter

OUTPUT VOLTAGE Va0	SWITCHING SEQUENCE							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
0	0	0	1	1	1	1	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{dc}/2$	1	1	1	1	0	0	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

A single-phase structure of an 5-level cascaded inverter is illustrated in Figure 2.2. Each separate dc source(SDCS) is connected to a single-phase full-bridge, or H-bridge,inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain+Vdc, switches S1and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2and S3. By turning on S1and S2or S3and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs[3]. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 5-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 2.2. The phase voltage van= va1+ va2+ va3+ va4+ va5.

III. Proposed Topology of Multilevel Inverter Circuit

The proposed inverter circuit is the single-phase five-level inverter. The schematic circuit of the proposedinverter is given below

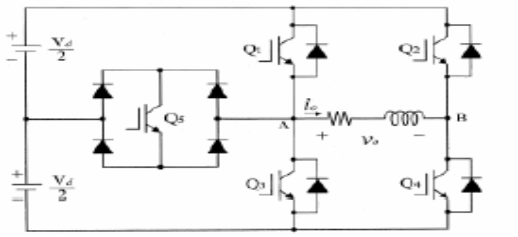


Fig.3.1 Configuration of the proposed single-phase five-level PWM inverter

Hence, the circuit topology shown in Fig.3.1 might be preferred not only under the aspect of harmonic content reduction due to several level of the output voltage as an essential feature of multilevel scheme, but also under the aspect of full utilization of semiconductor device in case that high voltage of dc-link could be applied.Output voltage and current harmonic content. Many different strategies for the multi-level pulse-width
modulation (PWM) exist.

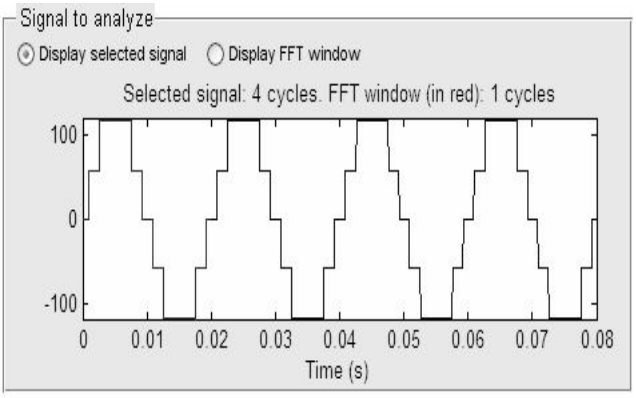
Usually the modulator is chosen to match the hardware topology. However, this choice does not always correspond to the PWM-strategy which generates the least harmonic content. This least- harmonics PWM-strategy can be used for all hardware topologies. It only requires a logic circuit to decode the PWM-output to the individual switch commands. Multilevel voltage-source inverters' unique structure allows them to span high voltages and to reduce individual device switching frequency without the use of transformers. Multi-level PWM inverters, (including five-level inverters), have significant operational advantage, such as the ability to drive a motor with nearly sinusoidal current waveforms and at higher output voltages[4].

The five level inverter has very simple commutation sequence which could make it possible to freely change output phase voltages between arbitrary two voltage levels, requiring no additional commutation circuitry.Commutation procedure between some levels should be divided into each one level commutation of unit change of voltage in order to guarantee voltage stress of both main switches and main diodes within unit level voltage Enduring transient time. One-level commutation can be carried out by first turning off the most upper (lower) main switch in one-state and turning on the opposite lower (upper) main switch in off-state after a required dead time. It should be noted that such commutation sequence facilitates utilization of switching devices even with different turn off times. Fig.3.1 shows a configuration of the proposed single-phase five-level PWM inverter. One switching -element and four diodes added in the conventional full-bridge inverter are connected to the center-tap of dc power supply. Proper switching control of the auxiliary switch can generate half level of dc supply voltage[5].

Fig.3.1 Operational states according to the switch on off conditions and the direction of load current. (a) State 1: vo= Vd , io = (+). (b) State 2: vo = Vd, io = (-). (c) State 3: vo =Vd/2, io = (+). (d) State 4: vo = Vd/2, io = (-). (e) State 5: vo = 0, io = (+). (f) State 6: vo = 0, io = (-). (g) State 7: vo = -Vd/2, io = (+). (h) State 8: vo = -Vd/2, io = (-).State 9: vo = -Vd , io = (+). (j) State 10: v = -Vd , i = (-).

The single-phase five-level PWM inverter whose output voltage has five values: zero, half and full supply dc voltage levels (positive and negative, respectively), so called a five-level single-phase PWM inverter

IV. RESULTS



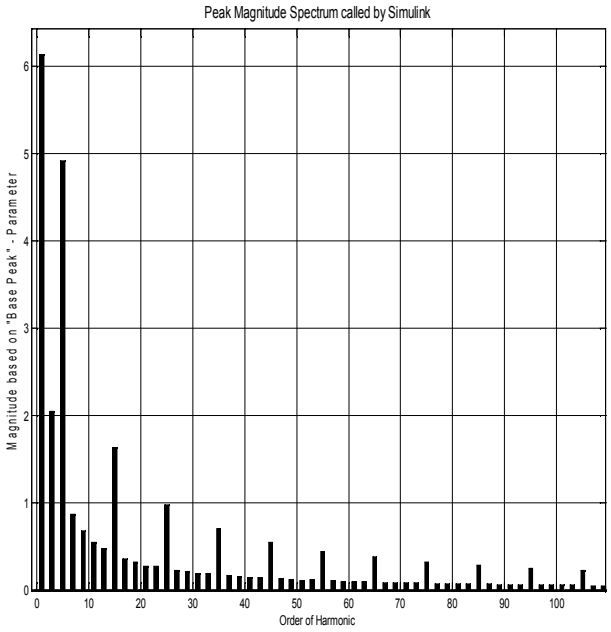


Fig 4.2(a) Proposed Topology for Continuous pulses & THD analysis

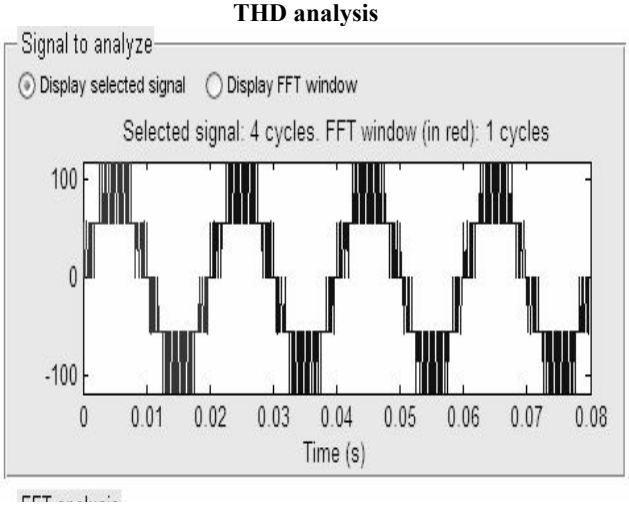
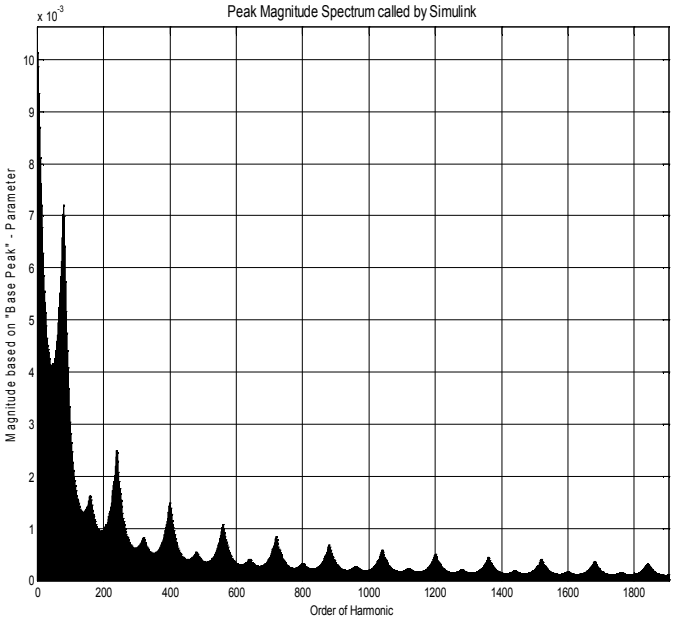


Fig 4.2(b) Multiple PWM pulses for Proposed topology of MLI & THD analysis



CONCLUSION

In this paper we have proposed we have new Modified cascaded topology for Multilevel Inverter. Thistopology reducing no. of switching devices as comparing with conventional cascaded multilevel inverter, i.e., for 5 level inverter it is reduced from 8 switching to 5 switching devices.

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