# Performance Analysis of Double Gate Tunnel Field Effect Transistor

**Shivesh Namdeo, Mr. Divyanshu Rao, Mr. Ravi Mohan**

***Abstract*— Here we have analyzed the impact of gate dielectric, device width, and metal electrodes on Tunnel Field Effect Transistor (TFET). A numerical T-CAD device simulator 3-D ATLAS version 2.10.18.R shows that reducing the width will reduce the effective threshold voltage. Transistor with high $I_{ON}/I_{OFF}$ ratio of $10^{11}$, sub-threshold swing of 42mV/decade for the channel length of 50nm with Hafnium oxide as gate dielectric material of thickness 3nm is considered. The performance analysis of Tunnel Field Effect Transistor is done by varying dielectric material, width of the device and varying the applied voltages. The simulation results indicate the suitability of proposed novel structure.**

***Index Terms*— Channel length, Hafnium, Sub-threshold swing, TFET, Tunneling**

## I. INTRODUCTION

Recent microelectronic trends, aim at the fabrication of the devices having nano scale dimensions. As the device dimension reduces, gate control on the channel charge carriers also reduces due to proximity of source and drain regions. The field and potential distributions in a small 3D field effect transistor deviates strongly from the often assumed 1D character, close proximity of electrodes not only adds to the capacitive loading of the active devices but also the parasitic capacitance. Parameters like threshold voltage, capacitance, $I_{ON}$ strongly depends on the geometric parameters. For this, alternative devices like tunnel field effect transistor (TFET) are reported in literature [7] and [8]. It is basically a heavily doped field effect transistor which uses the concept of tunneling, by narrowing the barrier between source and channel of the device, to turn the device ON and OFF. Simulation shows significant improvement compared to the simple metal oxide semiconductor field effect transistor. In the OFF state the current is in femto amperes. Decreasing the dimension will decrease the threshold voltage of the device however applied voltages were increased significantly.

It can be regarded as a novel device structure for use in high speed and low power electronic devices owing to its excellent Short Channel Effects, ideal sub-threshold swing, excellent gate controllability, low leakage current and good carrier transport efficiency.

Due to superior gate controllability, TFET can be used as the novel device in comparison to conventional MOSFET. Here, we have analyzed the impact of gate dielectric, width of the device and electrode contacts on the characteristics of TFET by using the procedure illustrated in [4] and [5], using numerical simulator 3D ATLAS version 2.10.18.R.

In section 2 we incorporate the device structure along with the simulation set-up. Simulation results and discussions about the characteristics of TFET are elaborated in section 3 and characteristics of various device parameters of TFET have been studied in section 4. Section 5 finally concludes the analysis of TFET.

## II. DEVICE STRUCTURE AND SIMULATION

Figure 1 shows device structure of reverse bias N-TFET. Gate length is 50 nm, source is 100nm, drain is 100nm, width is 5nm, device thickness is 10 nm, and gate electrode is surrounded by gate dielectric ($SiO_2$ or $HfO_2$) of thickness 3nm. Aluminum, Platinum and Hafnium electrodes are used as gate/source/drain contact on the top of silicon layer. 3D numerical device simulations are performed for proposed device using the device simulator 3D ATLAS version 2.10.18.R [3], [4] and [5]. The simulations are carried out using non local band-to-band tunneling model without impact ionization to account for highly doped channel, band-gap narrowing (BGN), Shockley Read Hall (SRH) recombination, Lombardi model and Auger recombination models. The mobility model includes both doping and transverse-field dependence. In Shockley Read Hall (SRH) recombination, generation and recombination are the major parameters which should be taken in consideration. Figure 1 and 2 elaborates the structure of the conventional and proposed structure of the tunnel field effect transistors respectively.

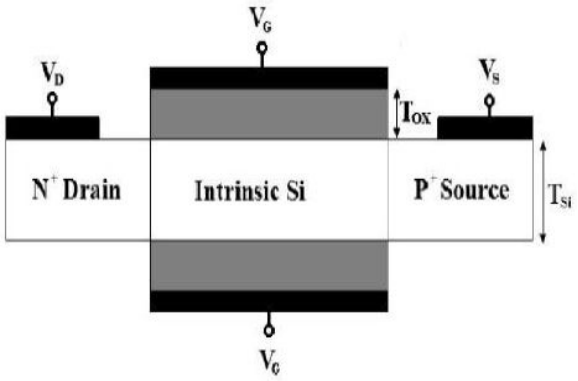


**Fig-1:** Conventional Tunnel Field Effect Transistor

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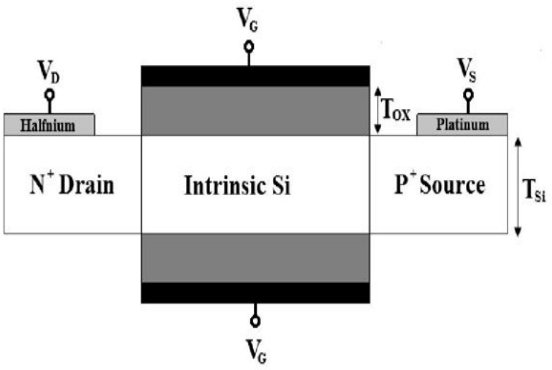


**Fig-2:** Proposed Tunnel Field Effect Transistor

**Table -I:** Parameters used during the device simulation

| PARAMETERS | T-FET |
|---|---|
| **Channel Length($L_g$)** | 50 nm |
| **Device layer Doping (Source p-type, channel p-type, drain n-type)** | $2.0 \times 10^{20} cm^{-3}$, $1.0 \times 10^{17} cm^{-3}$, $1.0 \times 10^{19} cm^{-3}$ |
| **Device layer thickness ($T_{Si}$)** | 10 nm |
| **Gate-Oxide material** | $SiO_2$ and $HfO_2$ |
| **Gate-oxide thickness ($t_{ox}$)** | 3 nm |
| **Gate Bias** | 0.0V to 3V |
| **Drain bias** | 1V to 2.5V |
| **Device width** | 5 nm to 40 nm |

## III. CHARACTERISTIC OF THE DEVICE

In this section, we have analyzed the various device characteristics of the TFET such as threshold voltage $V_{th}$, $I_{ON}/I_{OFF}$ ratio and sub-threshold swing (SS) by varying the device width, metal contacts, applied voltage and gate dielectric material. Figure 2 depicts the device with platinum electrode as source, hafnium electrode as drain and silicon dioxide as the gate dielectric material with doping concentration of source as $2.0 \times 10^{20}$ $cm^{-3}$, channel $1.0 \times 10^{17}$ $cm^{-3}$ and drain $1.0 \times 10^{19}$ $cm^{-3}$. Figure 3 shows threshold voltage ($V_{th}$) variations at the width of 5 nm, 10 nm, 15 nm, 20 nm, 25 nm and 30 nm. It is evident that with the increase in width, threshold voltage increases. $HfO_2$ is having, high $I_{ON}/I_{OFF}$ ratio of the two dielectric materials. Off current also reduces significantly by using $HfO_2$. Figure 5 depicts the SS variation at a particular width of Tunnel Field Effect Transistor of 5 nm dimensions taking gate dielectric $SiO_2$ and $HfO_2$. Table 2 elaborates the effect of various device parameters on device characteristics. It shows that $V_{th}$ and $I_{ON}/I_{OFF}$ decrease with the decrease in device width.

Using platinum at source and hafnium at drain side, there is an increase in ON current and if dielectric constant of gate oxide is increased then $V_{th}$ decreases and $I_{ON}$ increases. These parameters are taken as the reference parameters for comparing results with other TFETs and conventional CMOS devices. The gate capacitance and threshold voltage of the TFET increases due to the fringing effect and less dielectric surface area. The optimized simulation results of proposed device shows analyzed characteristics as compared with other TFET and conventional CMOS devices [7], [8] and [9]. For creating drain "n" with very high doping, hafnium (work function= 3.9 eV) is employed as the drain metal electrode. Similarly, for creating the "p" region with very high concentration platinum (work function= 5.93eV) is employed as the source metal electrode.

With the reduction in width of the device, fringing effect starts dominating because the channel length and width ratio starts to approach each other [9].

In circuits employing small geometry, parasitic capacitance becomes an appreciable fraction of the active device capacitance, this also slows down the circuit. A major fraction of the cross over capacitance, line capacitance and all the gate edge capacitances are related to fringing action. In tunnel field effect transistors if the channel length is reduced then threshold voltage reduces, because it reduces the barrier for flow of electrons and holes whereas when the device width is reduced threshold voltage decreases due to fringing action. Hafnium at the drain side provides very low resistance to the flow of electrons and hence provides higher concentration at the "n" side and also provides higher ON current due to very less resistance at the source channel region.

**Table -II:** Characteristic analysis

| **Parameters** | **Width of the device** ↓ | **Metal contacts work function** ↓ | **Dielectric constant** ↑ |
|---|---|---|---|
| **$V_{th}$** | ↓ | ↓ | ↓ |
| **$I_{ON}/I_{OFF}$** | ↓ | ↑ | ↑ |

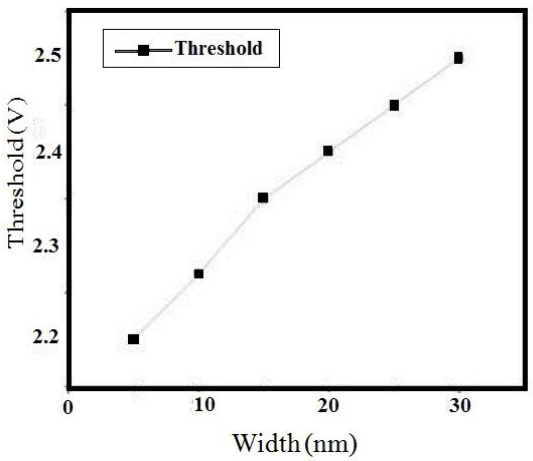


**Fig-3:** Threshold voltage ($V_{th}$) at different width

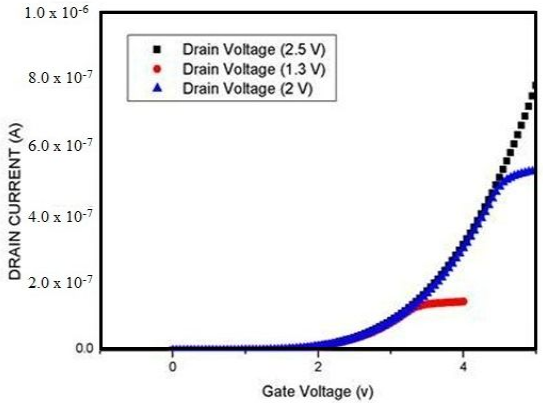


**Fig-4:** $I_{ON}/I_{OFF}$ at different applied voltages

## IV. CHARACTERISTICS OF VARIOUS DEVICE PARAMETERS

In this section, we have analyzed the various device parameters of TFET such as threshold voltage ($V_{th}$) by varying the device width. Table 3 depicts the percentage change in threshold variation with the change in width.

**Table -III:** Characteristic analysis

| N-Type TFET | Width increase by 5 nm |
|---|---|
| $\Delta V_{th}/V_{th}$ | 0.06 % □ |

Figure 5 shows the variations in parameters at different gate dielectric material and we observe that there is great effect on ON current of the device for high-K gate dielectric material which leads to more deviation in ON to OFF current ratio of the device. Table 3 shows the slight effect on the parameter with change in width (W) with dielectric material, indicating excellent control of the dielectric.

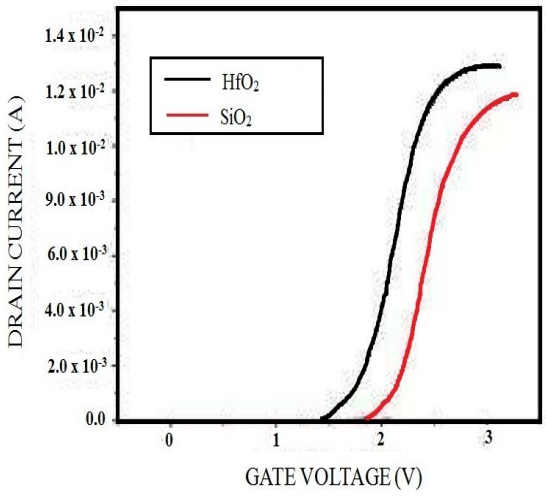


**Fig-5:** Characteristic analysis for Different gate dielectric materials

## CONCLUSION

Here we have analyzed that voltages applied are higher than the usual operation and the impact of gate dielectric, device width, metal contacts and channel engineering on characteristics of TFET by using numerical TCAD device simulator 3D ATLAS version 2.10.18.R [5]. The simulation results show high $I_{ON}/I_{OFF}$ current ratio with the applied voltages and increase in threshold voltage ($V_{th}$) with the increase in device width.

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