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Significance of Miller Indices on the Gate Threshold Voltage of NMOS at 90nm Technology

Yogita Dahiya, Bal Krishan

Abstract— **According to Moore's law "the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuits invented". In this paper we analyse MOSFET which is scaled down to 90nm and the threshold voltage with different crystallographic substrate orientation such as (100), (110) and (111). The results indicate that substrate orientation has a significant impact on threshold voltage. The proposed structure is scaled to 90nm and its threshold voltage and transconductance both are optimised to one substrate orientation**

***Index Terms*—Threshold Voltage, Transconductance, Retrograde channel doping, gate oxide thickness.**

I. INTRODUCTION

The metal oxide semiconductor field effect transistor (MOSFET), used in all analog and digital circuits, is generally used as amplifier and switches. For using MOSFETs in integrated circuits the dimension of MOSFET should be scaled. Nowadays the dimensions must be in nanometres. This technology has been around for many years and after many years of development the fabrication ways have also improved.

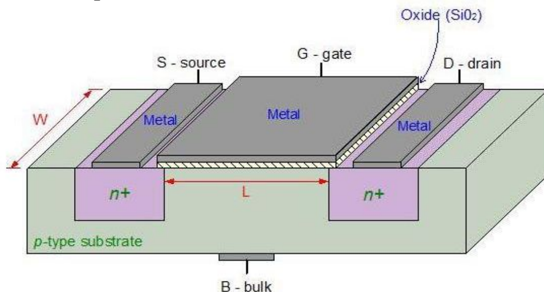

Fig 1: Basic structure of MOSFET

There are three main reasons to desire a small MOSFET:

A. Smaller MOSFET has small resistance so large current can flow.
B. Smaller MOSFET has small gate and therefore lower gate capacitances.
C. Smaller MOSFETs can be packed densely resulting in more transistors in same area.

With increasing the number of transistors on chip the transistor dimension decrease and the performance is improved. At dimensions of nanometres there are some factors which lead to increase in power dissipation and degrade the device performance. These factors are threshold voltage variation, drain induced barrier lowering, subthreshold swing, and current leakage also known as short channel effects.

The main objective is to develop the 90nm n-channel MOSFET (NMOS) for low power application and observe the effect of orientation or miller indices of silicon substrate on the gate threshold voltage.

II. MOSFET MODEL

When the channel of the MOSFET is scaled down to submicron regime, short channel effect will arise appear. These short channel effects are subthreshold leakage, Drain Induced Barrier Lowering, Punchthrough Current, Subthreshold Current, Gate Current. There are several advance technologies used to supress the short channel effect:

A. Retrograde channel doping: In this model we are using retrograde channel doping which implies that "The low surface concentration increases surface channel mobility by minimizing channel impurity scattering while the highly doped subsurface region acts as a barrier against punchthrough". The retrograde depth should transition from a low to high concentration very quickly. This reduces the threshold voltage and increase mobility.
B. Gate oxide thickness: Scaling gate oxide thickness also results in improved short channel effects.
C. Threshold voltage: "The voltage required to turn on the MOSFET is called the threshold voltage." As the gate voltage increases above the threshold voltage the MOSFET starts conducting as the electrons from substrate, source and drain starts accumulating and forms the sheet of charge called inversion layer. Due to the inversion layer electrons stay at higher energy level which widens the energy band gap. This further results in increased threshold voltage. In order to invert the channel, more band bending is required and voltage greater than classical voltage has to be applied at the gate terminal. This is called threshold voltage shift. This shift in threshold voltage is added to classical threshold voltage.

The gate to source voltage is given by [19]:

$$V_{gs} = V_{fb} + \phi_s + Q_s/C_{ox}$$

$$V_{gs} = V_{fb} + \phi_s + 2(\varepsilon_0\varepsilon_{si}qN_b\,\phi_s)^{1/2}/C_{ox}$$

and threshold voltage is,

$$V_T = V_{fb} + \phi_s + 2(\varepsilon_0\varepsilon_{si}qN_b\,\phi_f)^{1/2}/C_{ox}$$

Differentiating with respect to surface potential (ϕ_s), we get

$$dV_{gs}/d\,\phi_s = 1 + 0.5(\varepsilon_0\varepsilon_{si}qN_b)^{1/2}/(\phi_s)^{1/2}C_{ox}$$

Putting the condition $\phi_s = 2\,\phi_f$, we get

$$dV_{gs}/d\,\phi_s = 1 + 0.5(\varepsilon_0\varepsilon_{si}qN_b)^{1/2}/(\phi_f)^{1/2}C_{ox}$$

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Yogita Dahiya Department of electronics, YMCA University of Science and Technology, Faridabad, India

Bal Krishan Department of electronics, YMCA University of Science and Technology, Faridabad, India

Therefore, the shift in the threshold voltage is :

$$\frac{dVgs}{d\phi}\delta\phi s = \frac{dVt}{d\phi}\delta\phi s$$

III. FABRICATION STEPS

Fabrication steps comprises the modelling of all process steps which are necessary for the fabrication of any semiconductor device. Process steps include various layers of deposition, lithography, etching, implantation, oxidation and diffusion. The tool used for the simulation is SILVACO Athena, as a simulator it provides general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing [2].

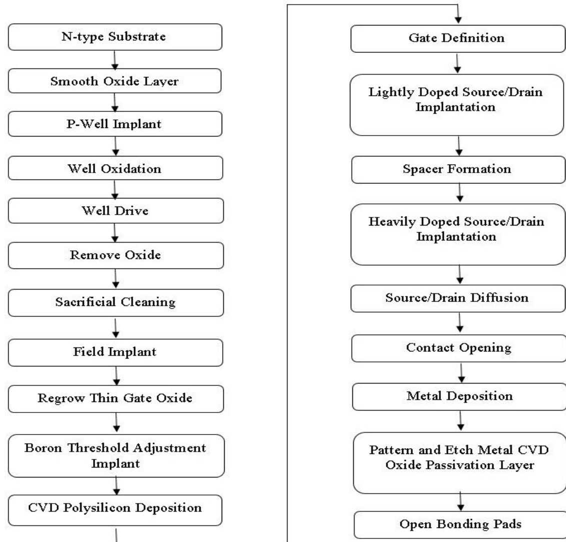

Fig 2: Basic NMOS fabrication flow chart

	Procedure	Process	Values
1	Formation of initial substrate	N-Type Substrate	P=1.0E14 cm^{-3} Orientation= <100>
2	Formation of P-Type well	Retrograde Well	B=5E12 cm^{-3} , E=300 KeV
3	Sacrificial oxide formation	Thermal oxidation	Thickness=25nm
4	Gate oxide thickness	Thermal oxidation	Thickness=2nm (20Å)
5	Vth adjust implant	Ion implantation	B=10E12 cm^{-3} , E=7 KeV
6	Polysilicon Silicon Deposition	Thin film deposition Lithography	Etch poly crystalline layer until 90nm is left
7	Source/Drain Extension(LDD)	Ion implantation	P=5E13 cm^{-3}, E=25KeV
8	Sidewall spacer formation	Thin film deposition	Thickness=120nm
9	Formation of Source/Drain Area	Ion implantation	Ar=2E16, E=40KeV
10	Annealing	RTA	1000C/3 sec.

Table 1: Process simulation using <100> oriented P-type substrate given B=>Boron, As=>Arsenic, P=>Phosphorous, E=>Energy

IV. PROPOSED DEVICE STRUCTURE

After all the processing steps of the NMOS fabrication, the results of the fabrication and simulation of 90 nm NMOS can be viewed in the Tony Plot, as shown below:

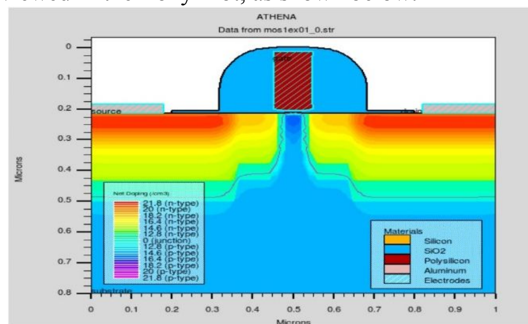

Figure 3: Complete structure of 90 nm NMOS <100>, <110> and <111>

As the device is scaled down, the threshold voltage reduces which means the power dissipation of the device also decreases. This implies that the device fabricated has low turn ON voltage and device is meeting the low power requirement. Therefore, device is having less propagation delay, so can be used in critical circuits. The parameters like transconductance and maximum drain current increases and this can be used to drive the high capacitive load.

At 90nm, at different orientation the threshold voltage and transconductance also varies with the substrate orientation. Every semiconductor has polarizable domain which align themselves in the direction of electric field. For best alignment with least amount of applied voltage there exist only one miller indices. Therefor threshold voltage shift in the crystal orientations (110) and (111) is larger as compared to (100) crystal orientations.

Parameters	285nm NMOS device (Default)	90nm NMOS device		
		100	110	111
Threshold Voltage	0.524 V	0.26516	0.3291	0.3236
Maximum Drain current	6xe^{-5} A	12xe^{-5}	12xe^{-5}	12xe^{-5}
Trans conductance	3.65xe^{-5}	8.72xe^{-5}	8.2 xe^{-5}	8.36 xe^{-5}

Table 2: Comparison of output parameters

CONCLUSION

The threshold voltage, with inversion layer quantization analytically derived, shows that crystal orientations also have a significant effect on the threshold voltage and inversion charge density of MOSFET at nanoscale levels.

Threshold voltage shift in the crystal orientations (110) and (111) is larger as compared to (100) crystal orientations. This shows the extent of impact of inversion layer quantization on the (110) and (111) crystal orientations making them less useful for the nanoscale MOSFETs.

The value of threshold voltage varies with the orientation of silicon substrate as stated in above comparison table. The orientation of <100> of silicon substrate has less threshold

voltage as compare to <110>, <111> orientation. The threshold voltage of <100> was found to be 0.265V which is in agreement with International Technology Roadmap for Semiconductor (ITRS) value, according to which Vth should be 0.268V±13% [3].

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Yogita Dahiya received B-tech degree in electronics and communication from Shri Mata Vaishno Dev University, India, 2013 and currently working towards her M-tech.

Bal Krishan received B-tech degree in electronics and communication and M-tech degree in nanotechnology.