High Performance Double Edge Triggered TSPC D Flip Flop

Latika Gulihar, Bal Krishan

***Abstract*— A memory element is the basic need of modern VLSI systems. If the performance of memory element is improved ultimately results in more reliable, robust and a high performance VLSI systems. Pulsed Clocked Double Edge Triggered Flip Flop (PDET) is proposed in this paper. PDET uses a new split output true single phase clocked (TSPC) and when clocked by a short pulse train act like a double edge triggered flip flop. Main focus of this paper are significant reduction in transistor count and number of clocked transistor. The number of transistor improves 56-60% compared to double edge triggered flip flop. Simulations are done using SEDIT in CMOS 180nm technology. The most important feature of this design is that it is suitable for both high speed and low power VLSI applications.**

***Index Terms*— PDET, TSPC, CMOS, VLSI, XNOR**

I. INTRODUCTION

The true single phase clock dynamic CMOS technique needs only one clock signal unlike other technique which requires inverted clock signal. Hence it has applications in both static and dynamic CMOS techniques. Advantage of this technique is elimination of skew due to different clock phases and clock signal being generated off chip, which results in significant reduction in area and power consumption. The generation and distributionof clock is not a factor of maximum sustainable clock frequency.

A single global clock is generated and distributed which simplify the design. The disadvantage of this design is the need of extra two transistors in each stage, a clock delay which can be eliminated by setting the value of clock delay less than the gate delay. Therefore it leads to more reliable design

The various advantages of TSPC are compact clock distribution, high speed, logic design flexibility, and robustness to reduce clock edges and eliminates the race hazards. In this section a single phase clocking scheme for high speed and compact VLSI digital systems is discussed. This structure is containing all components of digital VLSI system including static, dynamic, and precharge logic. The aim of this part is to discuss the existing solution using TSPC technique.

1.1 Pulse generation circuitry:

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The pulse generation circuit is composed of a XNOR block in first stage which consist of three transistors.

The purpose of this stage is to sample the signal on the positive and negative edge of the input square wave along with the delay of that clock. The delay is produced using an N-type TSPC split-output latch i.e proposed in this paper while keeping the clock constant at VDD and inverter is placed at the output .Next stage is a buffer that is composed of two inverter cells and having the same driving capability. The second stage is used as signal driver at the output of XNOR block. The circuit is depicted in Fig. 1. The

input of this circuit is a square wave clock signal with 50% duty cycle and short pulse train is generated as output of this circuit. In order to have a double edge-triggered flip-flop, the short pulse is produced on the positive and negative edge of the input clock as shown in [2]fig. 6

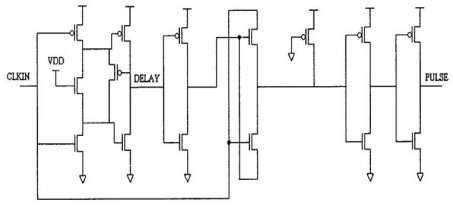

Fig 1: Pulse generation circuit

Implementation of Pulse generation circuit:

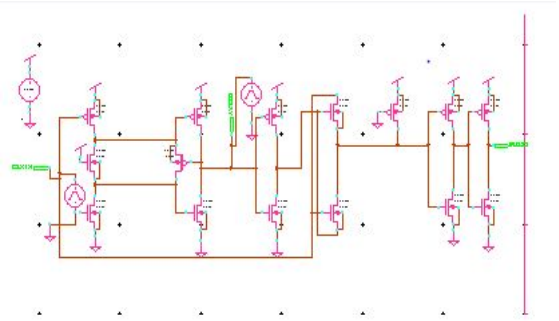

Fig 2: Implementation of Pulse clock generation

1.2 Comparison of TSPC Double Edge-Triggered Flip-Flop and PDET:

1.2.1 TSPC Double Edge-Triggered Flip-Flops

Previous double edge-triggered flip-flops were having two complementary latches in parallel. One latch was reacting on the positive edge and the other was reacting at the negative edge of the square clock pulse. Then using a merging circuit the output of the two latches were combined into a single output [6]. Within the merging circuit, when the output of the

one circuits is a high impedance node, it lets the other circuit decide the output value and vice-versa

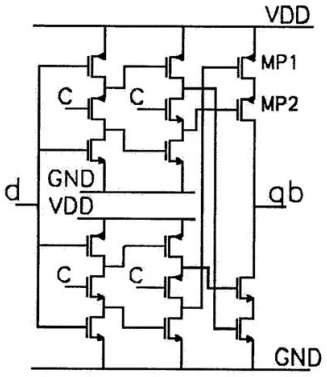

Fig 3: TSPC

1.2.2 PDET:

We are proposing a novel double edge-triggered pulse-clocked TSPC flip-flop(PDET) that uses only eight transistors. PDET is based on the TSPC split-output D-latch [8]. The N-type of this circuit that is used for double edge triggered flip -flop is depicted in fig 4. An Inverter has been added to the output of the original D latch to obtain true logic and not complementary logic.

The simple D latch circuit is shown in fig.4 when applied with the short pulse train clock generated by the pulse clock generator of fig 1, acts like a double edge-triggered flip-flop and is called, a pulse-clocked double D flip-flop (PDET).

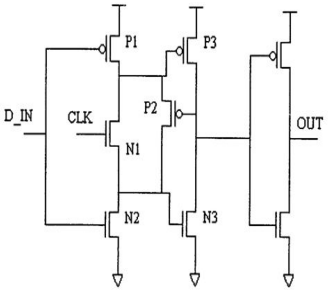

Fig 4: PDET

Implementation of PDET:

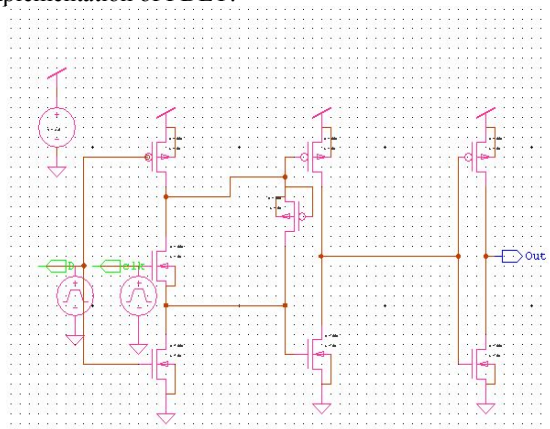

Fig 5: Implementation of PDET

II. SIMULATION AND RESULTS

Simulations have been performed using SEDIT and a 1.8 V power supply in a 0.18-µm CMOS process. For PDET simulations are performed on netlists extracted from layout. A simulation was performed for PDET circuit of fig. 5 using the same sizes for all transistors, W=5.4 µm and L=1.8 µm were used. The simulation was done using SEDIT in a 0.18 µm CMOS process. The power supply used is V_{DD}=1.8 V and the results of simulation are shown in fig.7. As seen in Fig.7, when clocked by the short pulse train generated by the pulse clock generator of fig. 6, the circuit does actually behave as a double edge-triggered flip-flop.

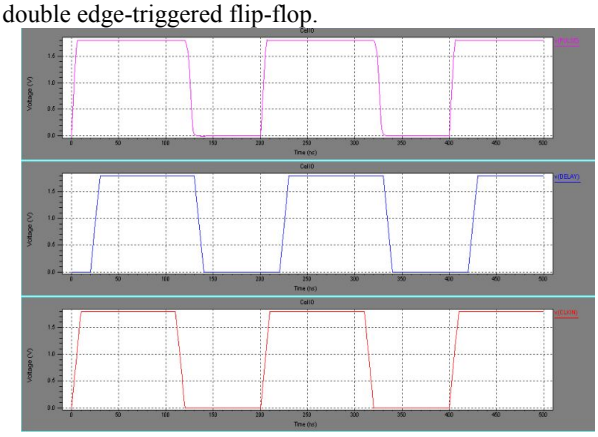

Fig 6: Output waveform of Pulse clock generation

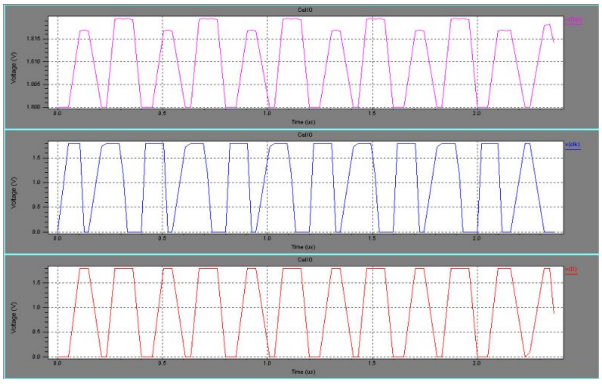

Fig 7: Output waveform of PDET

CONCLUSION

A new double edge triggered flip flop is introduced. The proposed double edge triggered flip flop is clocked with short pulse train and therefore called pulse clocked double edge triggered flip flop (PDET). The PDET is derived from a TSPC split output D Latch and use only eight transistors. The proposed PDET can save upto 60% in transistor count using 0.18µm CMOS technology. If optimzation with respect to geometry is applied it is possible to achieve much higher speed with the proposed .PDET keeping the power consumption low. It is concluded that proposed PDET seems to be more suitable storage element in high speed low power VLSI technology.

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