Design of Ultra-wideband LNA at operating frequency 4.1GHz with Current Reuse Techniques

Arun Sharma, Dr. R.P. Singh, Manish Kumar

***Abstract*— This paper presents an ultra-wideband (UWB) low noise amplifier (LNA) at operating frequency 4.1 GHz using a current-reused technique and source degeneration input matching network is proposed. The Implemented LNA presents a minimum Noise Figure of 1.069 dB at 4.1 GHz and the voltage gain obtained is 11.5dB.**

***Index Terms*—Noise Figure, Gain, UWB, Operating frequency, Current reuse**

I. INTRODUCTION

The proposed Ultra Wideband LNA is designed to operate at 4.1GHz frequency. LNA design is one of the challenges in radio frequency receivers, which needs a good input impedance match, and a low noise Figure (NF) within the required band or frequency. In this design current reuse topology [1] and source degeneration technique is used. The design is intended for narrowband application. The S parameters are used to characterize the performance of LNA. The S21 gives the value of gain for LNA, S11 tells about the matching at the input port, S22 gives the information about the matching at the output port and S12 is used to measure the reverse isolation. The noise figure is the ratio of SNR at input port to the SNR at the output port. For a good LNA, S21 should be as high as possible and S11 should be negative(in db) so that no power get reflect at the input port. For the maximum power at the output port, the S22 should also be negative (in dB). The current-reused configuration can be considered as a two stage cascade amplifier[3], where the first stage is the CS amplifier, and the second stage is the cascode amplifier and followed with an additional buffer stage at the output.

II. PROPOSED CIRCUIT DESIGN

The designed CMOS LNA circuit for UWB systems is shown in Fig. 1. The various components are connected in the circuits which helps in improving the performnace of LNA[4]. Inductor L2 is used for source degeneration technique so that input of M1 seems to be resistive which is given by

$$Z_n = Z_s + \frac{1}{sC_{gs}} + \frac{2sg_m}{sC_{gs}} \qquad (1)$$

Manuscript received May 11, 2016.

Arun Sharma, Electronics and Communication Engg., SSSIST,Sehore,Bhopal, M.P., INDIA
Dr. R.P. Singh, Electronics and Communication Engg., SSSIST,Sehore,Bhopal, M.P., INDIA
Manish Kumar, Electronics and Communication Engg., GLA University,Mathura,U.P.,INDIA

where Z_s is the parallel combination of $L_s \| C_{gd} \| r_{ds}$. By adjusting the value of frequency & L_s , the impedance can be made resistive. L_1 and C_1 are used for the impedance matching at the input port for low value of S_{11} or for transferring the maximum power.

The cascode topology has been used to reduce the reverse isolation means to reduce the load effect on the input impadance. Transistors M1 and M2 are connected in cascode with M1 as shown in Fig. 1. Shunt feedback topology has been used for increasing the stability of the circuit. By using the R1 as shunt feedback, the gain of the circuit get decreases so transistor M3 is connected in cascaded with M2 to provide the large gain.. The noise figure for an LNA circuit is given by

$$NF = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L} \qquad (2)$$

where
γ = Constant
α = Constant
R_S = Source Resistance
R_L = Load Resistance

The dependent current source will be equal to the MOFET transconductance with the v_{gs} i.e $g_m v_{gs}$ .The transconductance of MOSFET is given by

$$g_m = \frac{2I_D}{V_{OV}} \qquad (3)$$

$$\& \; V_{OV} = (V_{GS} - V_t) \qquad (4)$$

MOS Transistors M1 & M2 are connected in cascode form to achieve good input and output isolation; a parallel combination of inductor and capacitor (L3 ||C3) are used to pass the desired band of frequency. Transistor M3 is used in cascade with transistor M2 to increase the gain.

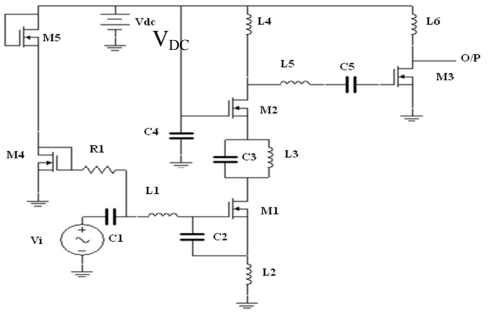

Fig.1 Proposed Circuit

Transistor M4 and M5 are used for biasing purpose; a combination of R1 and C1 is used as shunt feedback to the input signal to maximize the gain.
At the input inductor (L1),capacitor(C2) and inductor(L2) are used for better input impedance matching and inductor(L5),capacitor(C5) are set to achieve good gain and noise figure at desired frequency .

III. Simulation Results

The simulation results are shown in below figures. Figure2 shows the gain (S21) of the circuit; the result shows that at operating frequency 4.1 GHz gain is 11.5 dB.

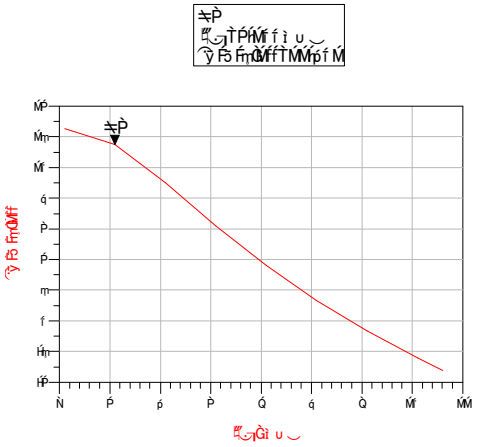

FIG. 2 Simulation Result for S21 vs RF Frequency

Figure 3 shows the simulation result for S11 which is -19.871 dB at operating frequency 4.1 GHz. High negative value of this parameter shows that the good impedance matching at input of the circuit.

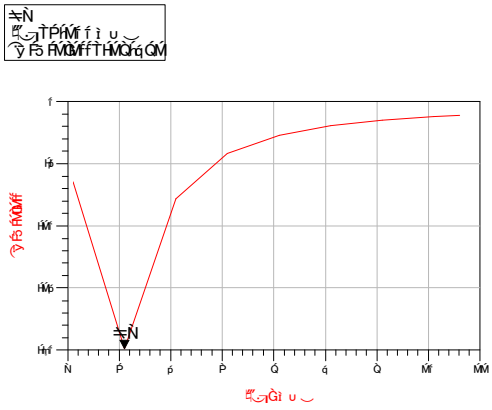

FIG. 3 Simulation Result for S11 vs RF Frequency

Figure 4 shows the simulation result for minimum noise figure for the circuit which is very good at operating frequency 4.1GHz and it's value is 1.069dB.

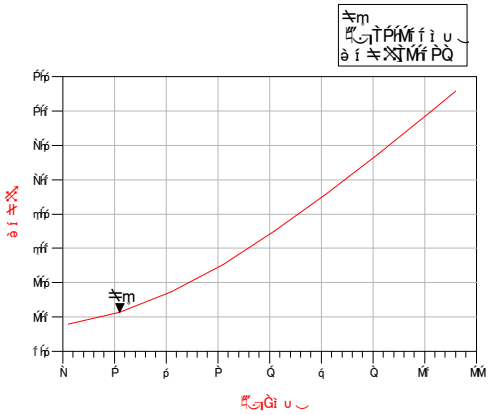

FIG. 4 Simulation Result for NFmin. vs RF Frequency

Figure 5 shows the simulation result for S12 with varying RF frequency. At operating frequency 4.1 GHz the S21 is -35.297 dB.

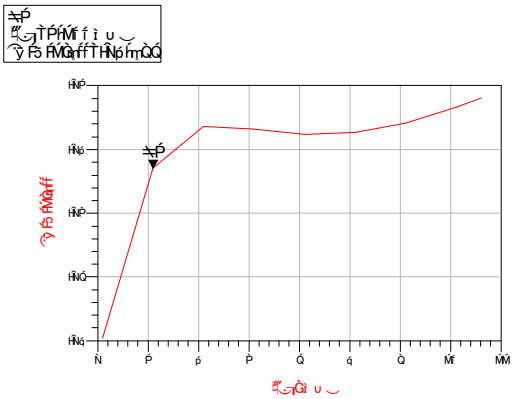

FIG. 5 Simulation Result for S12 vs RF Frequency

Conclusion

The CMOS LNA is proposed with 0.18µm technology. The value of gain is 11.5 dB at 4.1 GHz. The reflection at the input port is -19.87dB.The minimum value of noise figure is 1.069dB at 4.1GHz. The proposed circuit has cascade and cascode connection of transistors with current reuse technique and designed for narrowband applications.

References

[1] Pou-Tou Sun, Shry-Sann Liao, Hung-Liang Lin, Chung-Fong Yang, and Yu-Hsuan Hsiao," Design of 3.1 to 10.6GHz Ultra-wideband Low Noise Amplifier with Current Reuse Techniques and Low Power Consumption"in Progress In Electromagnetics Research Symposium, Beijing, China, March 23-27, 2009

[2] Lin, Y.-J., S. S. H. Hsu, Member, IEEE, J.-D. Jin, and C. Y. Chan, "A 3.1{10.6 GHz ultra- wideband CMOS low noise amplifier with current-reused technique," Digest of Technical

Papers, IEEE Microwave and Wireless Components Letters, Vol. 17, No. 3, Mar. 2007.

[3] Liu, R.-C., C. S. Lin, K.-L. Deng, and H. Wang, "A 0.5{14 GHz 10.6 dB CMOS cascade distributed amplifier," Digest of Technical Papers, 2003 Symposium on SI Circuits, 139{141,June 12{14, 2003.

[4] I-Chuan Chen; Jeng-Rern Yang, "3–10GHz CMOS distributed amplifier low-power and low-noise and highgain low noise amplifier for UWB systems," in TENCON 2010 - 2010 IEEE Region 10 Conference , vol., no., pp.2045-2047, 21-24 Nov. 2010

[5] Ismail, A. and A. A. Abidi, "A 3{10-GHz low-noise amplifier with wideband LC-ladder match-ing network," IEEE Journal of Solid-State Circuits, Vol. 39, Issue 12, 2269{2277, Dec. 2004.

Arun Sharma

Arun Sharma is pursuing M.Tech in VLSI Design from Sri Satya Sai Institute of Technology and Management affiliated to RGPV University Bhopal.

Dr. R.P. Singh

Dr. R.P. Singh is former Director and Prof. Electronics and Communication at Maulana Azad National Institute of Technology, (MANIT) Bhopal. Dr. Singh Graduated and Post Graduated in Electronic Engineering from Institute of Technology (now IIT), B.H.U. Varanasi in 1971 and 1973, respectively. He did his Ph.D. from Barakatullah University Bhopal in 1991. He has 39 years of teaching, research, and administrative experience in Maulana Azad College of Technology (MACT)/MANIT out of which 22 years as Professor. He was Head of the Department at of Electronics, and Computer Science and Engineering Department at MANIT Bhopal from Jan 1996 to April 1998 and again during 2005-2008. He has worked as Professor In-charge Academic and Chairman Admission Committee Dean (Academic) & Dean (R/D) at MACT /MANIT, Bhopal. He has published 125 papers in National / International reputed and indexed Journals including SCI. He has authored two books in the area of Communication Engineering; one of these books is published by MP Hindi Granth Academy in Hindi and other in English by TMH. He has worked as Secretary, Chairman, IETE, M.P. and C.G. and Council Member, IETE. He was first Counselor of IEEE student's chapter at MACT, Bhopal. He has been member of Executive Committee, Institution of Engineers (I) M.P. Circle. He was Chairman of Computer Society of India. Bhopal. He was member of Board of Studies, and Research Degree committee of many Universities. He has chaired Technical Sessions of various National and International Conferences. He has been Consulting Editor of Journal of Institution of Engineers and reviewer in many International/National Journals.

Manish Kumar

Manish Kumar is Asst. Professor at GLA University in Dept. of Electronics and communication Engineering. He is pursuing his Ph.D. from GLA university, Mathura. He has completed his M.Tech in VLSI Design from GBTU. He did B.Tech.(Electronics and Communication)from M.J.P. Rohilkhand University, bareilly (U.P.) .He has around 10 years of academic experience and published many research publications.