A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques

V. Raghuram Mahathi, R.Chander, M.Prudhviraj

***Abstract*— The high – voltage gain DC-DC boost converters are extensively employed in many industry applications, such as photovoltaic systems, fuel cell systems, uninterrupted power supplies, electric vehicles, and high-intensity discharge lamps. In the commonly employed conventional classical booster, the voltage stress of the main switch is equal to the high output voltage; hence, a high-voltage rating switch with high on-resistance should be used, generating high conduction losses. In addition, an extremely high duty cycle will results in large conduction losses on the power device and serious reverse recovery problems. As a result, the conventional boost converter would not be acceptable for realizing high step-up voltage gain along with high efficiency. In the present work, a novel single-switch high step-up non-isolated DC-DC converter integrating coupled inductor with extended voltage doubler cell and diode–capacitor techniques is proposed. The proposed converter achieves extremely large voltage conversion ratio with appropriate duty cycle and reduction of voltage stress on the power devices**

***Index Terms*— Coupled inductor, diode capacitor, Voltage gain**

I. INTRODUCTION

In recent years, high voltage gain dc–dc boost converters play more and more important role in many industry applications such as uninterrupted power supplies, electric traction, distributed photovoltaic (PV) generation systems, fuel cell energy conversion systems, automobile HID headlamps, and some medical equipments [1]–[18]. In these applications, a classical boost converter is normally used, but the voltage stress of the main switch is equal to the high output voltage; hence, a high-voltage rating switch with high on-resistance should be used, generating high conduction losses. In addition, an extremely high duty cycle will results in large conduction losses on the power device and serious reverse recovery problems. As a result, the conventional boost converter would not be acceptable for realizing high step-up voltage gain ($V_{out} \geq 8Vin$) along with high efficiency. Many non-isolated topologies have been researched to achieve a high conversion ratio and avoid operating at extremely high-duty cycle. These converters include the switched-capacitor types [10], [11], switched-inductor types [12], [13], the voltage-doubler circuits [15], [16], the voltage-lift types [14], [17], and the capacitor–diode voltage multiplier [18]–[20].All of them can present higher voltage gain than the conventional boost converter. However, more switched capacitor or switched-inductor stages will be necessary for an extremely large conversion ratio, resulting in higher cost and complex circuit. In this a novel single switch dc–dc converter with high voltage gain is presented.

The features of the proposed converter are as follows:

1) The voltage gain is efficiently increased by a coupled inductor and the secondary winding of the coupled inductor is inserted into a diode-capacitor for further extending the voltage gain dramatically;

2) A passive clamped circuit is connected to the primary winding of the coupled inductor to clamp the voltage across the active switch to lower voltage level. As a result, the power devices with low voltage rating and low on-state resistance $R_{DS}(ON)$ can be selected. On the other hand, this diode–capacitor circuit is useful to increase voltage conversion ratio;

3) The leakage inductance energy of coupled inductor can be recycled, improving the efficiency; and

4) The potential resonance between the leakage inductance and the junction capacitor of output diode may be cancelled.

The proposed converter's steady-state operational principles are given in Section II. The circuit performance analysis will be the aim of Section III, where an approximate dc analysis (losses neglected) is performed to get the static voltage gain and voltage stress on power devices. The key parameter design guidance is presented in Section IV.

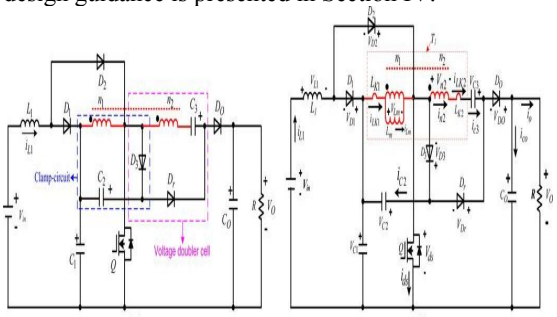

Fig.1.1. Circuit structure of the proposed converter

OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1.1(a) shows the circuit structure of the proposed converter, which consists of an active switch Q, an input inductor L_1 and a coupled inductor T_1, diodes D_1, D_2, and D_0, a storage energy capacitor C_1 and a output capacitor C_0 , a clamped circuit including diode D_3 and capacitor C_2 , an extended voltage doubler cell comprising regeneration diode D_r and capacitor C_3 , and the secondary side of the coupled inductor. The simplified equivalent circuit of the proposed

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converter is shown in Fig. 1.1(b). The dual-winding coupled inductor is modeled as an ideal transformer with a turn ratio N (n2 /n1), a parallel magnetizing inductance L_m, and primary and secondary leakage inductance L_{k1} and L_{k2}. In order to simplify the circuit analysis of the converter, some assumptions are as follows:

1) The input inductance L_1 is assumed to be large enough so that i_{L1} is continuous; every capacitor is sufficiently large, and the voltage across each capacitor is considered to be constant during one switching period;

2) All components are ideal except the leakage inductance of the coupled inductor;

3) Both inductor currents i_{L1} and i_{Lm} are operated in continuous conduction mode, expressed as C-CCM; the inductor current i_{L1} is operated in continuous conduction mode, but the current i_{Lm} of the coupled inductor is operated in discontinuous conduction mode, which is called C-DCM.

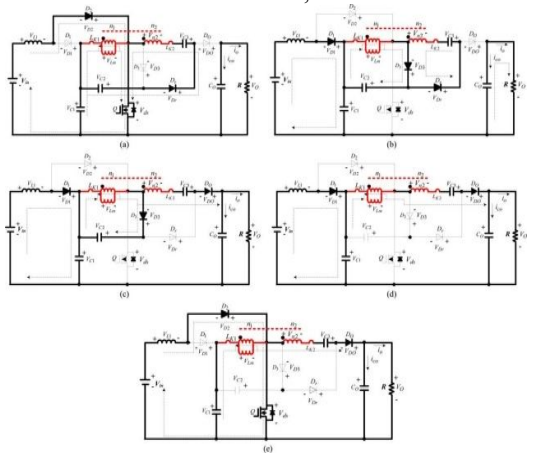

Fig.1.2. Equivalent circuits of five operating stages during one switching period at C-CCM operation

1.1 C – CCM

Based on the aforementioned assumption, the corresponding equivalent circuits are shown in Fig. 1.2. and Fig. 1.3. illustrates some key waveforms under C-CCM operation in one switching period, and The operating stages are described as follows:

Stage 1 [t_0 –t_1]: The switch Q is conducting at t = t_0 . Diodes D_1,D_3 ,and D_0 are reverse-biased by V_{C1}, V_{C1}+V_{C2} and V_0 – V_{C1} – V_{C2} , respectively. Only Diodes D_2 and D_r are turned ON. Fig.1.2.(a) shows the current-flow path. The dc source V_{in} energy is transferred to the inductor L_1 through D_2 and Q. Therefore, the current i_{L1} is increasing linearly. The primary voltage of the coupled inductor including magnetizing inductor L_m and leakage L_{K1} is V_{C1} and the capacitor C_1 is discharging its energy to the magnetizing inductor L_m and primary leakage inductor L_{K1} through Q. Then currents i_{D2}, i_{Lm}, and i_{K1} are increasing. Meanwhile, the energy stored inC_2 and C_1 is released toC_3 through D_r. The load R energy is supplied by the output capacitor C_0. This stage ends at t = t_1.

1) **Stage 2 [t_1 –t_2]:** In this transition interval, Fig. 1.2(b) depicts the current-flow path of this stage. Once Q is turned OFF at t = t_1 , the current through Q is forced to flow through D_3 . At the same time, the energy stored in inductor L_1 flows through diode D_1 to charge capacitor C_1 instantaneously and the current i_{L1} declines linearly. Thus, the diodeD_2 is reverse biased by V_{C2} . The diode D_0 is still reverse biased by V_0 – V_{C1} – V_{C2} . The energy stored in inductor L_{K1} flows through diodeD_3 to charge capacitor C_2. Therefore, the energy stored in L_{K1} is recycled to C_2. The i_{LK2} keeps the same current direction for charging capacitor C_3 through diode D_3 and regeneration-diode D_r. The voltage stress across Q is the summation of V_{C1} and V_{C2}. The load energy is supplied by output capacitors C_0 .This stage ends when i_{LK2} reaches zero at t = t_2.

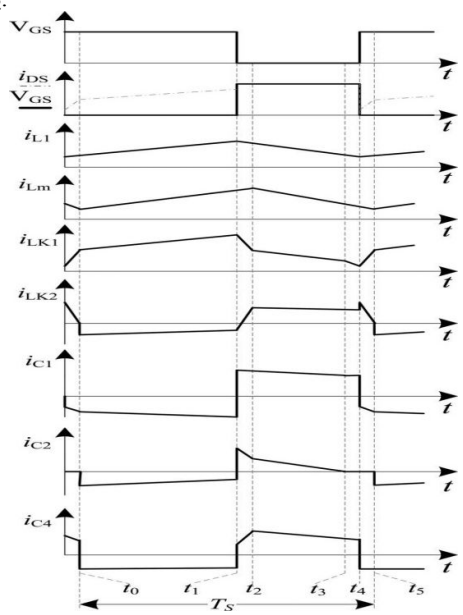

Fig. 1.3. The key waveforms of the proposed converter at C-CCM operation

2)

3) **Stage 3 [t_2–t_3]:** During this transition interval, switch Q remains OFF. Since i_{LK2} reaches zero at t = t_2, V_{C2} is reflected to the secondary side of coupled inductor T_1; thus, regeneration-diode D_r is blocked by V_{C3} + NV_{C2}.Meanwhile, the diode D_0 starts to conduct. Fig. 1.2(c) depicts the current-flow path of this stage. The inductance L_1 is still releasing its energy to the capacitor C_1. Thus, the current i_{L1} still declines linearly. The energy stored in L_{K1} and L_m is released to C_2 .Moreover, the energy stored in L_m is released to the output via n2 and C_3. The leakage inductor energy can thus be recycled, and the voltage stress of main switch is clamped to the summation of V_{C1} and V_{C2} . This stage ends when current i_{LK1} = i_{LK2}, thus the current i_{C2}= 0 at t = t_3.

Stage 4 [t_3 –t_4]: During this time interval, the switch Q, diodes D_2 and D_r is still turned OFF. Since i_{C2} reaches zero at t = t_3, the entire current of i_{LK1} flows through D_3 is blocked. The current-flow path of this mode is shown in Fig. 1.2(d). The energy stored in an inductor L_1 flows through diode D_1 to charge capacitor C_1 continually, so the current i_{L1} is decreasing linearly. The dc source V_{in}, L_1, L_m, L_{K1}, the winding n2, L_{K2} and V_{C3} are series connected to discharge their energy to capacitor C_0 and load R. This stage ends when the switch Q is turned ON at t = t_4.

Stage 5 [t_4 –t_5]: The main switch Q is turned ON at t_4 . During this transition interval, diodes D_1,D_3 , and D_r are reverse-biased by V_{C1}, V_{C1}+V_{C2} and V_0 – V_{C1} – V_{C2} , respectively. Since the currents i_{L1} and i_{Lm} are continuous, only diodes D_2 and D_0 are conducting. The current-flow path is shown in Fig. 1.2(e). The inductance L_1 is charged by input voltage V_{in}, and the current i_{L1} increases almost in a linear way. The blocking voltages V_{C1} is applied on magnetizing inductor L_m and primary-side leakage L_{K1}, so the current i_{Lk1} of the coupled inductor is increased rapidly. Meanwhile, the

magnetizing inductor L_m keeps on transferring its energy through the secondary winding to the output capacitor C_0 and load R. At the same time, the energy stored in C_3 is discharged to the output. Once the increasing i_{LK1} equals the decreasing current i_{Lm} and the secondary leakage inductor current i_{K2} declines to zero at $t = t_5$, this stage ends.

1.2 C – DCM

To simplify the C-DCM analysis, all leakage inductances of the coupled inductor are neglected. The coupled inductor is modeled as a magnetizing inductor L_m and an ideal transformer. The equivalent circuits for each subinterval are shown in Fig. 1.4.The key waveforms of the proposed converter are shown in Fig.1.5. There are four main stages during one switching cycle and detailed operation of each case is presented next.

Stage 1 [t_0 –t_1]: During this time interval, Q is turned ON. Diodes D_2 and D_r are conducted but diodes D_1, D_3, and D_0 are blocked by V_{C1}, $V_{C1}+V_{C2}$, and $V_0 - VC1 - V_{C2}$, respectively. The current-flow path is shown in Fig. 1.4(a). The inductance L_1 is charged by input voltage V_{in}; thus, the current i_{L1} increases linearly. The energy from capacitor C_1 transfers to magnetizing L_m and current i_{Lm} increases linearly. Meanwhile, capacitor C_3 is charged through the secondary winding coil n2 by capacitors C_1 and C_2. The output capacitor C_0 provides its energy to load R. The clamped diodeD_3 is biased forward when the main switch Q is turned OFF at $t = t_1$, and this stage ends.

Stage 2 [t_1–t_2]: At $t = t_1$, the switch Q is turned OFF, resulting in a current commutation between the switch Q and diode D_3 immediately. During this transition time interval, diodes D_2 and D_r are turned OFF because they are respectively anti biased by V_{C2} and $V_0 - V_{C1} - V_{C2}$, and other diodes are conducting. The current-flow path is shown in Fig. 1.4(b). The dc sources V_{in} is series-connected with inductor L_1 and transfer their energies to the capacitor C_1 through D_1 . The capacitors C_2 is charged by the magnetizing inductor L_m via D_3 . Similarly, the dc source V_{in}, inductor L_1, magnetizing inductor L_m and capacitor C_3 are series connected to transfer their energy to capacitor C_0 and load R. This stage ends when the rising current i_{C3} equals to current i_{Lm} at $t = t_2$. At the same instant, the diode D_3 is reverse biased at $t = t_2$

b)

a)**Stage 3 [t_2 –t_3]:** During this time interval, the switch Q, D_2 and D_r remain turned OFF. The diodes D_1 and D_0 are still turned ON. Since i_{C2} reaches zero at t_2 , the coupled inductor transfers energy to the output, and diode D_3 is also blocked. The current-flow path is shown in Fig. 1.4(c). The dc source V_{in} and the input inductor L_1 are still connected serially to charge capacitor C_1 . Thus, the current i_{L1} continues to decrease. Meantime, the primary and secondary sides of doubled-inductor are serially connected, and serially connected with V_{C3}, delivering their energy to the output capacitor C_0 and load R. This stage ends when the current i_{Lm} reduces to zero at $t = t_3$.

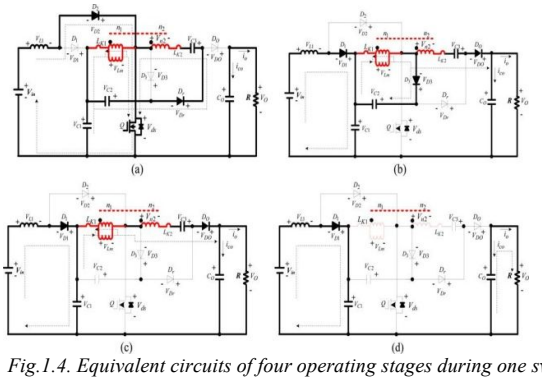

Fig.1.4. Equivalent circuits of four operating stages during one switching period at DCM operation

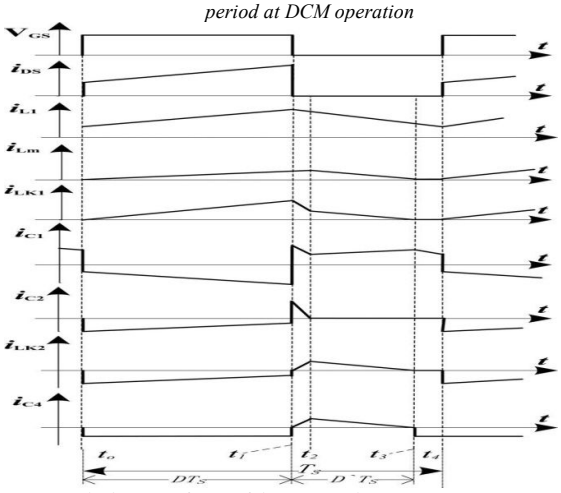

Fig.1.5. The key waveforms of the proposed converter at C-DCM operation

Stage 4 [t_3 – t_4]: During this transition time interval, the switch Q and the diode D_2 is still turned OFF. Meanwhile, the primary and secondary currents of the coupled inductor have run dry at t_3. Therefore, the diode D_3 is still blocked by $V_{C1}+V_{C2}$, and only diode D_1 is conducting for continuous i_{L1}. The current-flow path is shown in Fig. 1.4(d). The capacitor C_1 is still charged by the energy stored in L_1 and dc sources V_{in}. Since the energy stored in L_m is empty, the energy stored in C_0 is discharged to load R. This stage ends when Q is turned ON at $t = t_4$, which is the beginning of the next switching period.

II. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

2.1 C-CCM Operating Conduction

To simplify the analysis, the leakage inductances of the coupled inductor are neglected in the steady-state analysis. Also, the losses of the power devices are not considered. Only stages 1 and 3 are considered for C-CCM operation because the time durations of stages 2, 4, and 5 are short significantly. At stage1, the main switch *Q* is turned ON, the inductor L_1 is charged by the input dc source V_{in}, and the magnetizing inductor L_m is charged by the voltage across C_1. The following equations can be written from Fig. 3.2(a):

$$V_{L1}=V_{in} \quad (1)$$

$$V_{Lm}=V_{C1}. \quad (2)$$

And the voltage of the switched capacitorC_3 can be expressed by

$$V_{C3}=NV_{C1}+V_{C1}+V_{C2} \quad (3)$$

During stage 3, the main switch Q is in the OFF state, the inductor L_1 and magnetizing inductor L_m are discharged, respectively. The voltages across the inductor L_1 and L_m can be obtained by

$V_{L1}=V_{in}-V_{C1}$ (4)

$V_{Lm}=-V_{C2}$ (5)

$V_0=V_{C1}+(N+1)V_{C2}+V_{C3}$. (6)

Using the inductor volt-second balance principle to the inductor L_1 and magnetizing inductor L_m, the following equations can be expressed as:

$$\int_0^{DT_s} V_{in}\,dt+\int_{DT_s}^{T_s} V_{in}-V_{C1}\,dt=0 \quad (7)$$

$$\int_0^{DT_s} V_{C1}\,dt+\int_{DT_s}^{T_s} -V_{C2}\,dt=0 \quad (8)$$

From (1)–(8), the voltages across capacitors C_1, C_2, and C_3 are derived as follows:

$$V_{C1}=\frac{V_{in}}{1-D}=\frac{(1-D)V_0}{2+N} \quad (9)$$

$$V_{C2}=\frac{DV_{in}}{(1-D)^2}=\frac{DV_0}{2+N} \quad (10)$$

$$V_{C3}=\frac{(N+1-DN)V_{in}}{(1-D)^2}=\frac{(N+1-DN)V_0}{2+N} \quad (11)$$

Substituting (9)–(11) into (6), dc voltage gain MC-CCM is obtained as

$$M_{C-CCM}=\frac{V_0}{V_{in}}=\frac{2+N}{(1-D)^2} \quad (12)$$

Fig. 2.1 demonstrates the relationships between the voltage gain and the duty cycle in the conventional quadratic boost converter, reference [32] converter, and the proposed converter at CCM operation. One can see that the proposed converter can realize higher voltage gain with the same duty cycle and turns ratio of the coupled inductor. According to the description of the operating stages and neglecting the voltage ripple on the clamp capacitor, the maximum voltage stress of the main switch can be derived by

$$V_{stress-Q}=\frac{V_0}{2+N} \quad (13)$$

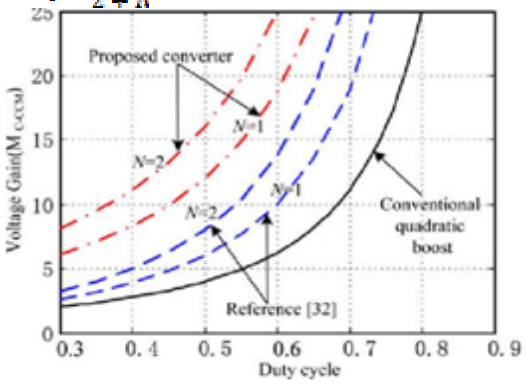

Fig. 2.1. Voltage gain comparison of the proposed converter, the conventional quadratic boost and reference [32] converter.

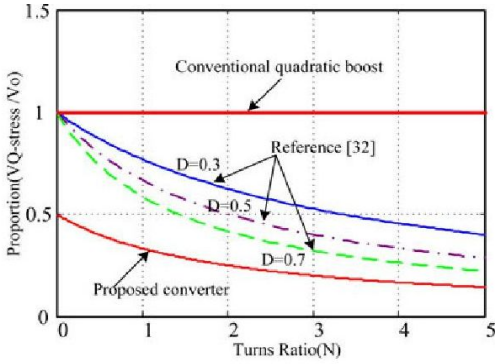

Fig. 2.2. Voltage stress reduction comparison of the main switch

The comparison of the main switch voltage stresses between the conventional quadratic boost converter, reference [32] converter, and the proposed converter is shown in Fig. 4.2.In the conventional quadratic boost converter, the voltage stress of the main switch always equals to the output voltage. The main switch voltage stress of reference [32] is determined by duty cycle and the turn ratio of the coupled inductor, which is far lower than the output voltage with increasing duty ratio. Fortunately, the voltage stress of the main switch in the proposed converter is only determined by the turn ratio of the coupled inductor and the output voltage. One can see that the voltage stress of the switch decreases sharply with increasing turns ratio. Thus, the high-performance active switch can be used here to improve the efficiency. The voltage stress on the diodes are given by

$$V_{stress-D1}=\frac{V_{in}}{1-D}=\frac{(1-D)}{2+N}V_0 \quad (14)$$

$$V_{stress-D2}=\frac{DV_{in}}{(1-D)^2}=\frac{D}{2+N}V_0 \quad (15)$$

$$V_{stress-D3}=\frac{V_{in}}{(1-D)^2}=\frac{1}{2+N}V_0 \quad (16)$$

$$V_{stress-D0}=\frac{(1+N)V_{in}}{(1-D)^2}=\frac{(1+N)}{2+N}V_0 \quad (17)$$

$$V_{stress-Dr}=\frac{(1+N)V_{in}}{(1-D)^2}=\frac{(1+N)}{2+N}V_0 \quad (18)$$

In terms of the operating principles, the current ripples on the input inductor and magnetizing inductor are expressed as

$$\Delta I_{L1}=\frac{DT_sV_{in}}{L_1} \quad (19)$$

$$\Delta I_{Lm}=\frac{DT_sV_{C1}}{L_m} \quad (20)$$

Since the average currents of i_{C2}, i_{C3}, and i_{C0} are zero in the steady state, the average currents that flow through D_r,D_0 and the magnetizing inductor are, respectively, equal to the average value of i_0. The current stresses on power devices are can be derived as

$$I_{D1(Peak)}=I_{L1}+\frac{\Delta I_{L1}}{2} \quad (21)$$

$$I_{D2(Peak)}=I_{L1}+\frac{\Delta I_{L1}}{2} \quad (22)$$

$$I_{D3(Peak)}=I_0+\frac{DT_sV_{C1}}{2L_m} \quad (23)$$

$$I_{Dr(Peak)}=\frac{2I_0}{D} \quad (24)$$

$$I_{D0(Peak)}=\frac{2I_0}{1-D} \quad (25)$$

$$I_{Q(Peak)}=I_{D1(Peak)}+I_{Lm(Peak)}=I_{L1}+\frac{\Delta I_{L1}}{2}+I_0+\frac{DT_sV_{C1}}{2L_m} \quad (26)$$

When the switch Q is OFF, the average current stresses which flow through capacitors C_1 and C_3 can be estimated as

$$I_{C1(off)} = I_{L1} \approx \frac{2+N}{(1-D)^2} I_0 + \frac{DT_s(1-D)^2 V_0}{2L_1(2+N)} \quad (27)$$

$$I_{C3(off)} = I_0 \quad (28)$$

By using the ampere-second principle on capacitors C_1 and C_3 , the following equations can be expressed as:

$$\int_0^{DT_s} I_{C1(on)}\,dt + \int_{DT_s}^{T_s} I_{C1(off)}\,dt = 0 \quad (29)$$

$$\int_0^{DT_s} I_{C3(on)}\,dt + \int_{DT_s}^{T_s} I_{C3(off)}\,dt = 0 \quad (30)$$

Substituting (27), (28) into (29) and (30), the following equations are derived when the switch Q is ON:

$$I_{C1(on)} \approx \frac{2+N}{D(1-D)} I_0 + \frac{DT_s(1-D)^2 V_0}{2L_1(2+N)D} \quad (31)$$

$$I_{C3(on)} = I_{C2(on)} \approx \frac{1-D}{D} I_0 \quad (32)$$

According to the current-balance principle on capacitor C_2, the following equation can be expressed as:

$$\int_0^{DT_s} I_{C2(on)}\,dt + \int_{DT_s}^{T_s} I_{C2(off)}\,dt = 0 \quad (33)$$

The average current stress on the capacitor C_2 is approximated as the switch Q is OFF

$$I_{C2(off)} = I_0 \quad (34)$$

2.2 C-DCM Operating Condition

In C-DCM operation, there are four stages. The key waveforms are shown in Fig. 1.5. During the time of stage 1, the switch Q is turned ON, and only diodesD_2 and D_r are turned ON. The following equations can be written as:

$$V_{L1}=V_{in} \quad (35)$$

$$V_{Lm}=V_{C1} \quad (36)$$

$$V_{n2}=NV_{Lm}=V_{C3}-V_{C2}-V_{C1} \quad (37)$$

During the time of stage 3, switch Q is turned OFF, and only diodes D_1 andD_0 are conducting. The voltage levels across inductorL_1 and magnetizing L_m and secondary winding coil $n2$ are given as follows:

$$V_{L1}=V_{in}-V_{C1} \quad (38)$$

$$V_{Lm} = \frac{V_{C3}+V_{C1}-V_0}{N+1} \quad (39)$$

$$V_{n2} = \frac{N(V_{C3}+V_{C1}-V_0)}{N+1} \quad (40)$$

During the time of stage 2, the output voltage V_0 can be expressed as

$$V_0=V_{C1}+V_{C3}+(N+1)V_{C2} \quad (41)$$

If $D\_$ is defined as the duty cycle of the magnetizing inductor current from peak point ramped down to zero. By applying the volt-second balance principle to the inductor L_1, magnetizing inductor L_m and the secondary side of winding coil $n2$, the following equations are derived:

$$\int_0^{DT_s} V_{in}\,dt + \int_{DT_s}^{(D+D')T_s} V_{in} - V_{C1}\,dt = 0 \quad (42)$$

$$\int_0^{DT_s} V_{C1}\,dt + \int_{DT_s}^{(D+D')T_s} \frac{V_{C3}+V_{C1}-V_0}{N+1}\,dt - 0 \quad (43)$$

$$\int_0^{DT_s} (V_{C3}-V_{C1}-V_{C2})\,dt + \int_{DT_s}^{(D+D')T_s} \frac{N(V_{C3}+V_{C1}-V_0)}{N+1}\,dt = 0 \quad (44)$$

From (38)–(44), the voltages of C_1, C_2, C_3 , and $D\_$ are obtained

$$V_{C1} = \frac{V_{in}}{1-D} \quad (45)$$

$$V_{C2} = \frac{DV_{in}}{(1-D)D'} \quad (46)$$

$$V_{C3} = \frac{[(N+1)D'+D]V_{in}}{(1-D)D'} \quad (47)$$

$$M_{C-DCM} = \frac{V_0}{V_{in}} = \frac{(2+N)(D+D')}{(1-D)D'} \quad (48)$$

$$D' = \frac{D(2+N)V_{in}}{V_0(1-D)-(2+N)V_{in}} \quad (49)$$

The peak value of magnetizing inductor current I_{LMP} is expressed by

$$I_{Lmp} = \frac{DT_sV_{C1}}{L_m} = \frac{DT_sV_{in}}{L_m(1-D)} \quad (50)$$

Since the average currents through capacitors C_2, C_3, and C_0 are zero in a steady state, the average current values of i_{D3}, i_{Dr}, and i_{Do} are, respectively, equal to the average of I_0 , and

$$I_{D2} = I_{Dr4} = I_{D0} = \frac{D'I_{Lmp}}{2} = I_0 \quad (51)$$

Since $I_0 = V_0 /R$, substituting (50) and (51) into (49) obtains the voltage gain of the proposed converter in C-DCM as follows:

$$M_{C-DCM} = \frac{V_0}{V_{in}} = \frac{(2+N)+\sqrt{(2+N)^2+2D^2(2+N)\frac{R}{L_m f_s}}}{2(1-D)} \quad (52)$$

Where *fs* is the switching frequency.

BCM Operating Condition

If the input current through L_1 of proposed converter is operated in boundary-condition mode, the boundary inductor L_{1B} can be derived as

$$L_{1B} = \frac{D(1-D)^2R}{2(2+N)^2 f_s} \quad (53)$$

When the current through L_m of the proposed converter is operated in boundary-condition mode, the boundary magnetizing inductor L_{mB} can be depicted by

$$L_{mB} = \frac{D(1-D)^2R}{2(2+N)f_s} \quad (54)$$

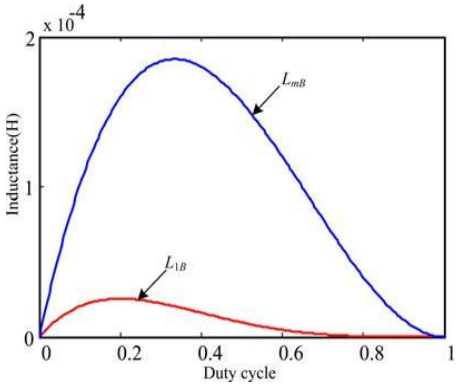

Fig. 2.3. Boundary condition of the proposed converter with N = 2.

The relationship between the L_{1B} and the duty cycle, the load, the switching frequency, and the turn ratio are plotted in Fig. 4.3. Once the L_1 is higher than L_{1B} , the inductor L_1 will be

operated in the continuous conduction mode. As shown in Fig. 2.3, if the L_m is larger than L_{mB}, the coupled inductor will be operated in the continuous conduction mode. In the practical application, one can make a micro adjustment.

III. KEY PARAMETER DESIGN GUIDANCE

3.1 Input Inductor L_1 Selection

For renewable dc low-voltage sources such as PV array or fuel cell, the lower input current ripples are usually required, so the design guidance of the proposed converter employed in C-CCM is given, and the input inductor L_1 is designed to make that the input current ripple is approximately 15% of the average input current, which is derived by

$$L_1 = \frac{DV_{in}}{\Delta I_{L1} f_s} \qquad (55)$$

3.2 Turns Ratio and Magnetizing Inductor of Coupled Inductor Selection

In the proposed converter, the coupled inductor stores energy like an inductor. Therefore, the coupled inductor should be designed like a fly-back transformer. The turns ratio of the coupled inductor determines the switch duty cycle, and the voltage, current stresses of power devices, which is obtained by

$$N = \frac{V_0}{V_{in}}(1-D)^2 - 2 \qquad (56)$$

If the switch duty cycle is selected, the turns' ratio of the coupled inductor can be calculated and the power device voltage/current stress can be easily carried out. As a result, the power devices will be chosen easily by considering some acceptable voltage and current margins. Usually, the duty cycle should be less than 0.7 to reduce conduction loss of the converter. However, if the duty ratio is too small, the increasing turn ratio will lead to larger volume of the coupled inductor and boundary magnetizing inductance. Furthermore, the bigger magnetic core leads to more energy loss. As a result, a compromise should be made to optimize the turns ratio of the coupled inductor for a given voltage gain. In practical applications, the turn ratio from 1 to 3 is more appropriate for the proposed converter. In this project, the designed feature of the proposed converter is mainly operated in C-CCM. In practical applications, the theoretical boundary magnetizing inductance can be designed at 30–45% full load by equation (54).

3.3 Active Switch and Diodes Selection

The voltage/current rating of the active components can be obtained from (13)–(18), and (21)–(26). In practice, voltage spike usually could be produced during switch transition process because of the effect of the leakage inductance and parasitic capacitor. Besides, the spike voltage also could be generated due to stray inductance and capacitance existing in practical PCB.Therefore, regarding the aforementioned effects of the circuit and traces, the voltage/current rating of the selected power devices will usually be more than 150% of the calculated value

3.4 Considerations of the Capacitor Design

To suppress the voltage ripple on the clamp capacitor C_2 and the switched capacitor C_3 to a tolerant range is main consideration. Hence, the estimated capacitances depend on the equations (57) and (58).Where ΔV is the maximum tolerant voltage ripple on the capacitors C_1, C_2, C_3, or C_0

$$C \geq \frac{2P_{max}}{V_C^2 f_s} \qquad (57)$$

$$C \geq \frac{2P_{max}}{V_C \cdot \Delta V_C \cdot f_s} \qquad (58)$$

In practice, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases, so the capacitor is usually selected to be larger than the calculated value during converter operation.

3.5 Analysis of Theoretical Efficiency

Once the major components' parameters are chosen, the efficiency of the converter can be estimated based on considering the parasitic resistive components. Some specific variable symbols of all parasitic components are assumed as follows: r_{L1} is the ESR of the input inductor L_1 ; r_{N1} and r_{N2} represent ESR of the primary and secondary windings of the coupled inductor; r_Q is the on-state resistance of the switch Q; r_{C1}, r_{C2} , and r_{C3} denote, respectively, the ESR of capacitors C_1, C_2 , and C_3 ; V_{FD1}, V_{FD2},V_{FD3},V_{FD4}, and V_{FD5} are the forward voltage drop of D_1,D_2,D_3,D_4 , and D_5 , respectively; r_{D1}, r_{D2}, r_{D3}, r_{D4} , and r_{D5} are, respectively, the forward resistance of D_1,D_2,D_3,D_4 , and D_5 . According to previous work [28], [36], the theoretical efficiency is found by

$$\eta = \frac{1 - A_3}{1 - A_2 + A_2 - A_4 + A_5}$$

$$A_1 = \frac{(1-D)}{(2+N)V_{in}}[(2+2ND+D^2-ND^2-D)V_{FD1}+(N-2D)V_{FD2}+V_{FD3}+V_{FD4}+V_{FD5}]$$

$$A_2 = \frac{(2-N)}{(1-D)^2R}[(N-2D)(r_{L1}+r_{N1})+(N-2D-2ND-D^2+ND^2-1)r_Q-(2ND+D^2-ND^2+2-D)(r_{L1}+r_{N1})]$$

$$A_3 = \frac{(2-N)}{(1-D)^2R}[(2D_{T1})+D(1+2N+D-ND)(r_{N1}+r_{C1}+r_T)+(1-D)(r_T-r_{C1}+2r_{N1})]$$

$$A_4 = \frac{1}{DR}[(2D-N)r_T+D(1+2N+D-ND)(r_{C1}+r_T)+(1-D)(r_{C2}+r_{C3}+r_{N2}+r_T-r_{C1})]$$

$$A_5 = \frac{r_{N2}+r_{C3}+r_{D4}}{R}+\frac{(2+N)D(1+2ND+D^2-ND^2)r_{C1}}{(1-D)^2R}+\frac{r_{C2}+r_{D3}}{R}$$

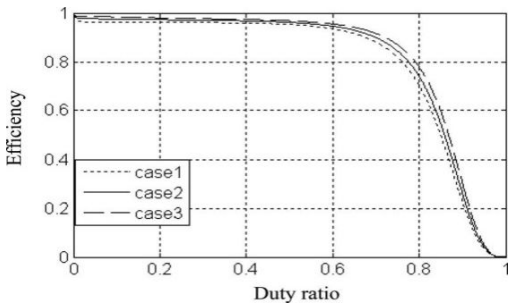

Fig. 3.1. Calculated efficiency η versus duty cycle for different parameters

Fig. 3.1 plots the calculated efficiency under three operating conditions. One can see that the theoretical efficiency is improved slightly with increasing turns ratio of the coupled inductor. But the efficiency will be decreased dramatically when the duty ratio is larger than 0.7. Therefore, the turn ratio can be designed as higher as possible under appropriate duty cycle range if only efficiency is desired. However, it should be noticed that the increasing turn ratio will result in larger volume of the coupled inductor and boundary magnetizing inductance. Furthermore, the bigger magnetic core leads to more energy loss. As a result, a compromise should be considered to optimize overall the system's performance.

IV. RESULTS AND DISCUSSIONS

4.1 Parameters considered:

The following parameters are considered for the proposed converter

1) TABLE 6.1

Components	Parameters
Input voltage V_{in}	20V
Switching frequency f_s	40 KHZ
Magnetizing inductor L_m	200µH
Leakage inductor L_{K1}/L_{K2}	1.7 µH
Input inductor L_1	60 µH
Power MOSFET Q	FQP34N20
Dr/Do Diodes	FFPF20U50
$D_1/D_2/D_3$(Diodes)	20ETF02
C_1(capacitor)	470 µF /100v
C_2(capacitor)	47 µF /100v
C_3(capacitor)	47 µF /250v
C_0(capacitor)	470 µF /600v

4.2 SIMULATION DIAGRAM

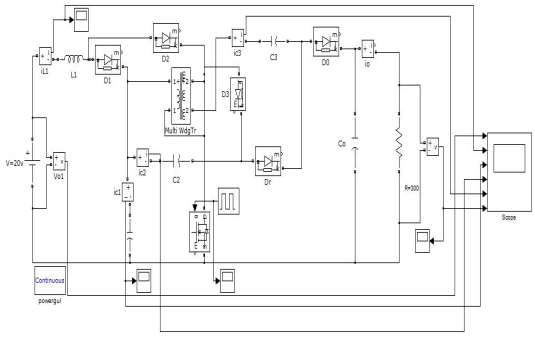

Fig.4.1. Simulation Diagram of Proposed Converter

The simulation is performed for various duty ratios and for different turns' ratio to clearly understand their effect on the performance of the converter.

4.3 SIMULATION RESULTS

The following are the various voltages and currents obtained across the network elements when duty cycle is 0.5 and transformation ratio 13/7.

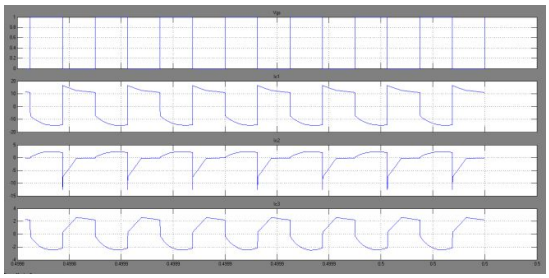

Fig.4.2.Waveforms of V_{in}, I_{L1}, I_{C1}, I_{C2},I_{C3},V_0 in C-CCM

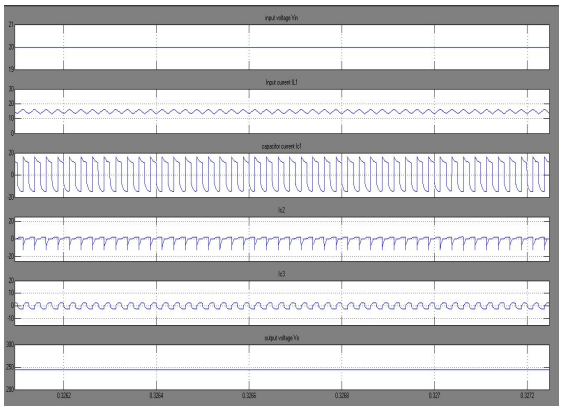

Fig.4.3.Waveforms of V_{gs} ,I_{C1}, I_{C2},I_{C3}, in C-CCM

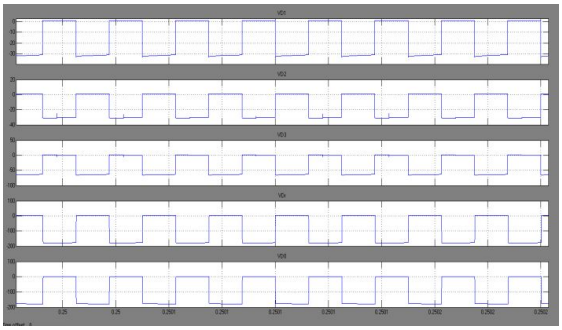

Fig.4.4.Voltage stress of Diodes V_{D1}, V_{D2}, V_{D3}, V_{Dr}, V_{D0} in C-CCM

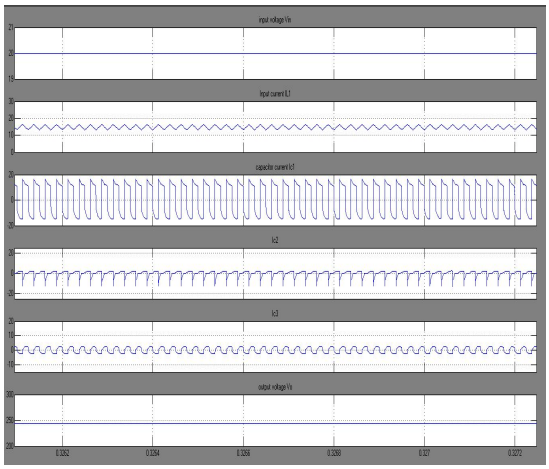

Fig.4.5.Waveforms of V_{in}, I_{L1}, I_{C1}, I_{C2}, I_{C3}, V_0 in D-CCM

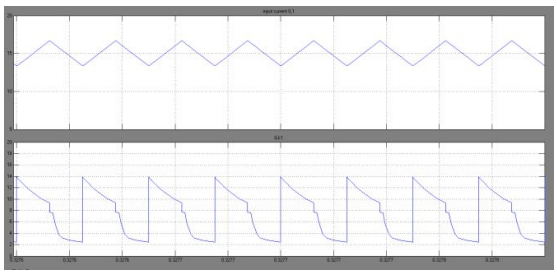

Fig.4.6Waveforms of I_{L1}, I_{LK1}, in D-CCM

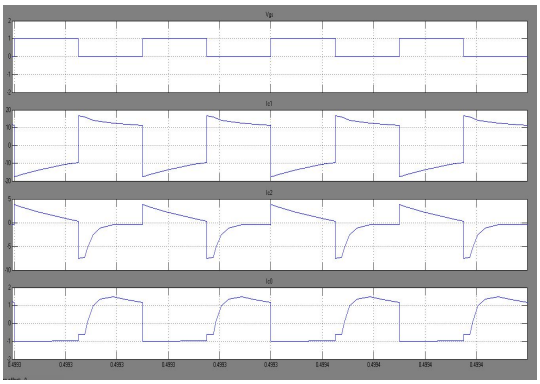

Fig.4.7.Waveforms of V_{gs} ,I_{C1}, I_{C2},I_{C0}, in D-CCM

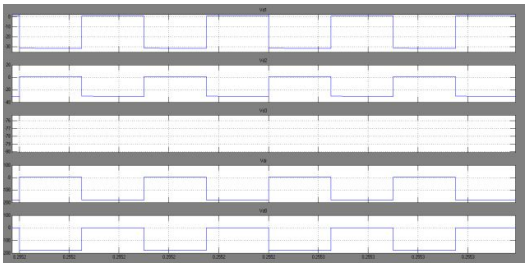

Fig.4.8.Voltage stress of Diodes V_{D1}, V_{D2}, V_{D3}, V_{Dr}, V_{D0} in D-CCM

CONCLUSION

For non isolated high step-up industry applications, a novel high-voltage gain converter is introduced in this paper, which combines a quadratic boost converter with coupled inductor and diode–capacitor techniques. A clamped-capacitor circuit is connected to the primary side of the coupled inductor, the voltage stress of the active switch is reduced greatly and the clamped capacitor also transfers the primary leakage energy to the output. At the same time, a diode-capacitor circuit is integrated with the secondary winding for further extending the voltage gain greatly. Furthermore, the energy of secondary leakage inductor can be recycled and the turned off voltage spikes on the main switch are suppressed. In addition, compared with some active clamp or three-level counterparts, only one MOSFET is required to simplify the circuit configuration and improve the system reliability, and the proposed converter maintains the advantage of continuous input current.

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