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New Breed of Single Phase Asymmetrical Multilevel Inverter

V. Arun, B. Shanthi, S.P. Natarajan

Abstract— **This paper presents a new breed of single phase asymmetrical multilevel inverter. The proposed inverter has less number of power semiconductor switches and sources than the conventional multilevel inverters. It is triggered by the Unipolar PWM strategy having sinusoidal and trapezoidal reference with triangular carriers. These Pulse Width Modulating (PWM) strategies include Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD), Carrier Overlapping (CO). Performance factors like Total Harmonic Distortion (THD), VRMS (fundamental), crest factor, Distortion factor and Form factor are evaluated for various modulation indices. Simulations were performed using MATLAB-SIMULINK**

Index Terms— THD, UAPOD, UCO, UPD, UPWM

I. INTRODUCTION

Multilevel inverters are power electronic systems that synthesizes a desired output voltage from several levels of dc voltages as inputs and multilevel inverters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Babaei et al [1] developed asymmetrical multilevel converters with reduction of DC voltage sources and switches. Dixon and Moran [2] proposed high-level multistep inverter optimization using a minimum number of power transistor. Hongyan et al [3] introduced novel carrier-based PWM methods for multilevel inverter. Naziha and Yatim [4] developed modular structured multilevel inverter for high power AC power supply applications. Pablo et al [5] described cascaded multilevel inverter with regeneration capability and reduced number of switches. Rodriguez et al [6] made a survey on multilevel inverter topologies, controls and applications. Sergio et al [7] introduced multilevel inverter topologies for stand-alone PV systems. Sung et al [8] developed a novel hybrid multilevel inverter using DC-link voltage combination. Takahashi and mochikawa [9] proposed A new control of PWM inverter for minimum loss operation of an induction motor drive. Tolbert and Thomas [10] described novel multilevel inverters using carrier based PWM methods. Yan et al [11] described multilevel PWM methods based on control degrees of freedom combination and its theoretical analysis. Zhong et al [12] introduced a cascade multilevel inverter using a single DC source. This paper presents a new breed of single phase asymmetrical DC source seven level inverter topology for investigation using unipolar PWM control strategies. Simulations were performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

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II. Asymmetric Cascaded Multilevel Inverter Proposed Multilevel Inverter

In case of asymmetric cascaded inverters, the H-bridge units are fed by unequal DC sources. The use of multiple DC sources can demand long cables and may lead to voltage unbalance among the sources. So, asymmetric cascaded inverters are used to provide a large number of output voltage levels without increasing the number of full bridge units. This configuration provides higher voltage at higher modulation frequencies due to which the topology can be employed for high power applications. Due to the reduction in the number of DC sources employed the structure becomes more reliable. Also, the output voltage has higher resolution due to the increase in the number of steps and the reference sinusoidal voltage can be better achieved.

III. Proposed Multilevel Inverter

The proposed inverter differs from conventional inverters. Fig. 1 shows a circuit configuration of a new breed of single phase asymmetrical DC source seven level inverter. The voltage levels are $0V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$. Each of the separate voltage source V_{dc} and $2V_{dc}$ connected in cascade with other sources via H bridge circuit associated with it. The basic operation is to turn on S1 and S2 (D turn off) and the output voltage is $+1V_{dc}$, turning on S2 and D (S1 turn off) producing output $+2V_{dc}$. Similarly other step can be achieved by turning on the suitable switches at particular intervals; Table.1 shows the basic operation of proposed new breed of multilevel inverter clearly.

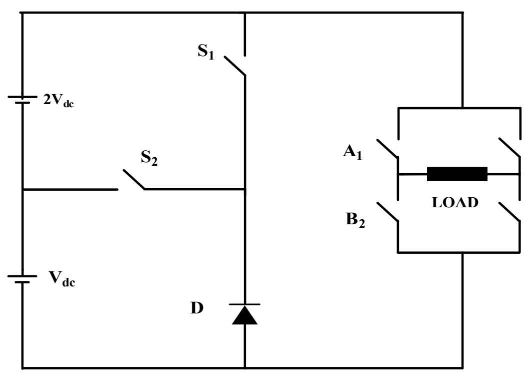

Fig. 1. New breed of Asymmetrical DC source MLI

In asymmetrical DC source MLI, output voltage level is seven, if *n* number of H-bridge module has independent DC sources in sequence of the power of 2, an expected output voltage level is given as

$$V_n = 2^{n+1} - 1, n = 1, 2.. \quad (1)$$

IV. Unipolar Pulse Width Modulation Scheme

The scheme uses a unipolar sine and trapezoidal as modulating signal and triangular as carriers. In this PWM scheme, triangular carriers are compared with rectified sine and trapezoidal reference. The intersection between the unipolar reference signal and the carrier signals defines the switching instant of the PWM pulse. The multiple carriers used are positioned above zero level and the number of carriers is dependent on the output voltage levels. For an m-level inverter, (m-1)/2 carriers with the same frequency f_c and the same amplitude A_c are disposed. The reference waveform has peak-to-peak amplitude A_m and frequency f_m. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

There are many alternative strategies are possible, some of them are tried in this paper and they are:

a. Unipolar Phase disposition PWM strategy (UPDPWM).

b. Unipolar Alternate phase opposition disposition PWM strategy (UAPODPWM).

c. Unipolar Carrier overlapping PWM strategy (UCOPWM).

The formulae to find the Amplitude of modulation indices are as follows:

For UPDPWM,

$$m_a = 2A_m/(m-1)A_c) \quad (2)$$

For

UCOPWM: $m_a = A_m / (2 * A_c)$ (3)

The frequency ratio m_f are as follows:

$$m_f = f_c / f_m \quad (4)$$

A) Unipolar Phase Disposition PWM (UPDPWM)

The triangular carriers of same amplitude and frequency are disposed such that bands they occupy are contiguous. The carrier arrangement for asymmetrical DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in figures 2 & 3 respectively

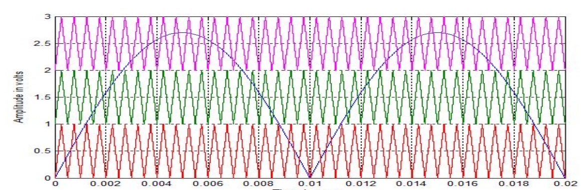

Fig. 2. Carrier arrangement for UPDPWM strategy with sinusoidal reference (ma=0.9 and m_f=40)

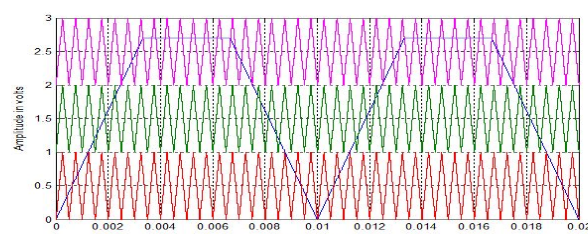

Fig. 3. Carrier arrangement for UPDPWM strategy with Trapezoidal reference (m_a=0.9 and m_f=40)

B) Unipolar Alternative Phase Opposition Disposition PWM (UAPODPWM)

Carriers for asymmetrical DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in figures 4 & 5 respectively. The triangular carriers of same amplitude are phase displaced from each other by 180 degrees alternately.

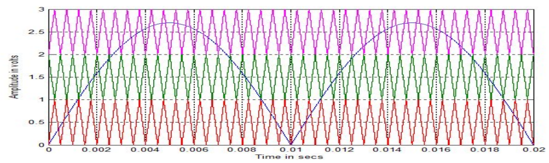

Fig. 4. Carrier arrangement for UAPODPWM strategy with sinusoidal reference (m_a=0.9 and m_f=40)

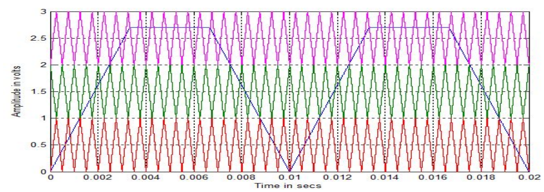

Figure. 5. Carrier arrangement for UAPODPWM strategy with Trapezoidal reference (m_a=0.9 and m_f=40)

C) Unipolar Carrier Overlapping PWM (UCOPWM)

Carriers for asymmetrical DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in figures 6 & 7 respectively. In carrier overlapping technique, carriers of same amplitude and frequency are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$.

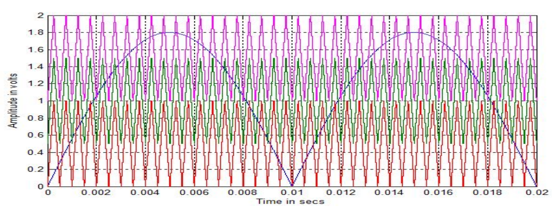

Fig. 6. Carrier arrangement for UCOPWM strategy with sinusoidal reference(m_a=0.9 and m_f=40)

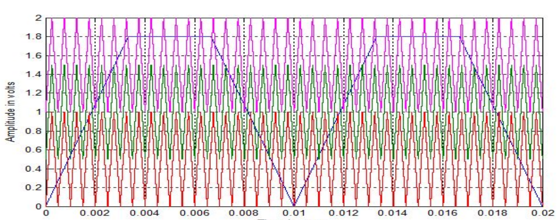

Fig. 7. Carrier arrangement for UCOPWM strategy with Trapezoidal reference (ma=0.9 and mf=40)

V. Simulation Result

The single phase asymmetrical DC source seven level inverter is modeled in SIMULINK using power system block set. Switching signals for asymmetrical multilevel inverter using UPWM strategies are simulated. Simulations were performed for different values of ma ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table I. Next table displays the V_{RMS} of fundamental of inverter output for same modulation indices. Table III and IV display respectively the corresponding Crest Factor (CF) and Distortion Factor (DF) of the output voltage. Fig. 8 (a) and (b) respectively shows the seven level output voltage generated by UPDPWM strategy with Sinusoidal reference and its FFT plot. Fig. 9 (a) and (b) respectively shows the seven level output voltage generated by UPDPWM strategy with Trapezoidal reference and its FFT plot. Fig. 10 (a) and (b) respectively shows the seven level output voltage generated by UAPODPWM strategy with Sinusoidal reference and its FFT plot. Fig. 11 (a) and (b) respectively shows the seven level output voltage generated by UAPODPWM strategy with Trapezoidal reference and its FFT plot. Fig. 12 (a) and (b) respectively shows the seven level output voltage generated by UCOPWM strategy with Sinusoidal reference and its FFT plot. Fig. 13 (a) and (b) respectively shows the seven level output voltage generated by UCOPWM strategy with Trapezoidal reference and its FFT plot.

The following parameter values are used for simulation: V_{DC} =100 V, R (load) = 100 ohms, f_c=2000 Hz and f_m=50Hz.

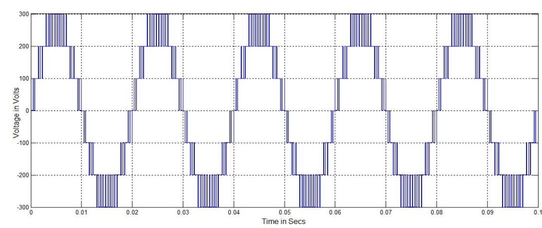

Fig. 8 (a). Output voltage generated by UPDPWM strategy with Sinusoidal reference

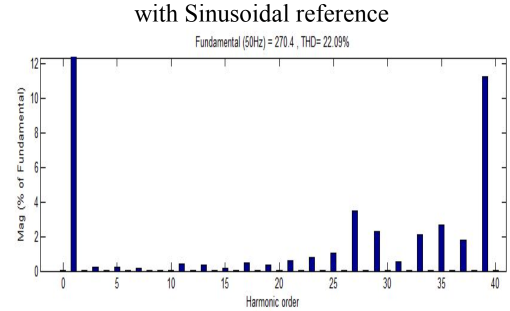

Fig. 8 (b). FFT plot for output voltage of UPDPWM strategy with Sinusoidal reference

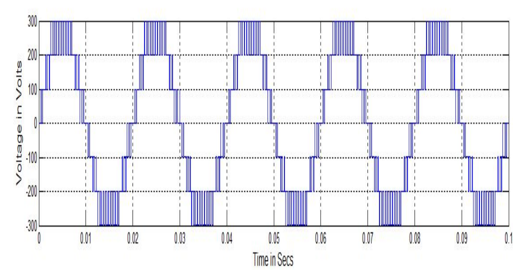

Fig. 9 (a). Output voltage generated by UPDPWM strategy with Trapezoidal reference

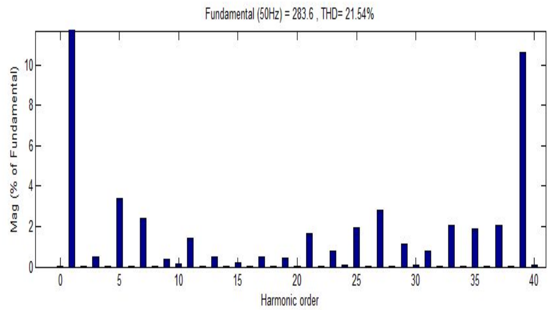

Fig. 9 (b). FFT plot for output voltage of UPDPWM strategy with Trapezoidal reference

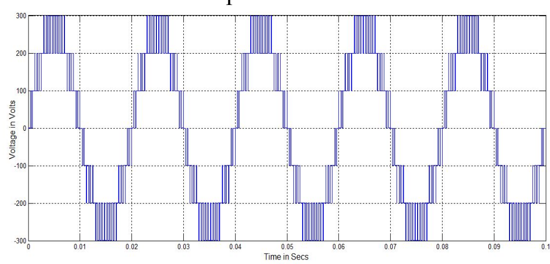

Fig. 10 (a). Output voltage generated by UAPODPWM strategy Sinusoidal reference

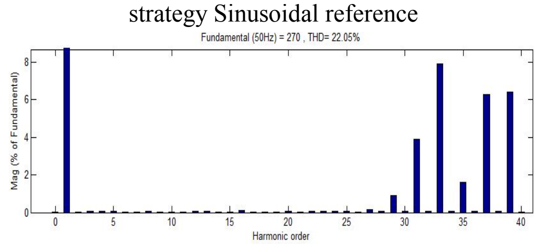

Fig. 10 (b). FFT plot for output voltage of UAPODPWM strategy with Sinusoidal reference

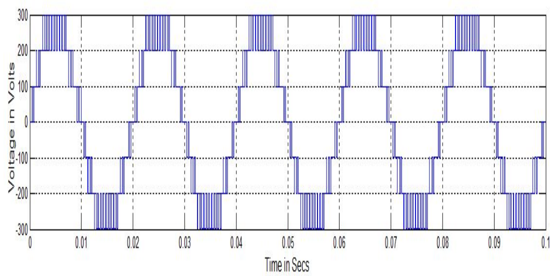

Fig. 11 (a). Output voltage generated by UAPODPWM strategy Trapezoidal reference

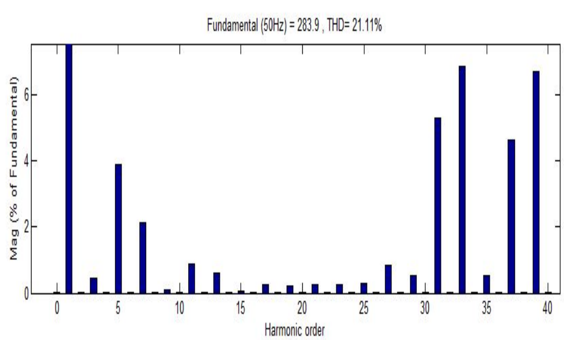

Fig. 11 (b). FFT plot for output voltage of UAPODPWM strategy with Trapezoidal reference

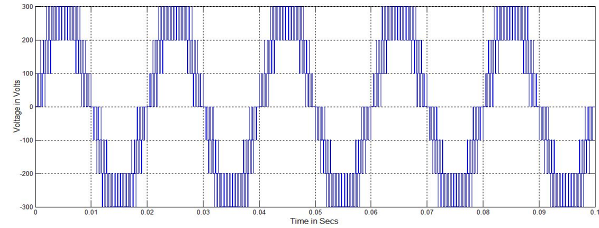

Fig. 12 (a). Output voltage generated by UCOPWM strategy with Sinusoidal reference

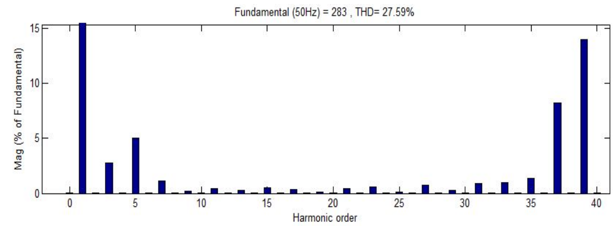

Fig. 12 (b). FFT plot for output voltage of UCOPWM strategy with Sinusoidal reference

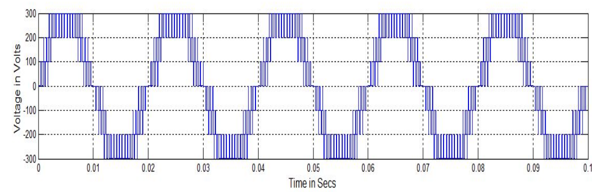

Fig. 13 (a). Output voltage generated by UCOPWM strategy with Trapezoidal reference

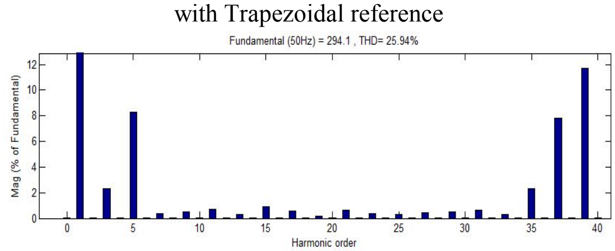

Fig. 13 (b). FFT plot for output voltage of UCOPWM strategy with Trapezoidal reference

It is observed from Table I, that the harmonic content of output voltages is least with UPDPWM and UAPODPWM strategy with trapezoidal reference provides relatively lower %THD for most of m_a. From Table II, it is found that UCOPWM strategy with trapezoidal reference provide higher DC bus utilization. CF is relatively equal for all the strategies (Table III). DF is relatively low in UPDPWM strategy with sinusoidal reference. (Table IV). FF is relatively equal for all the strategies (Table V).

For m_a= 0.9, it is observed from the Figure. (8 (b), 9 (b), 10 (b), 11(b), 12 (b), and 13 (b)) the harmonic energy is dominant in: a) 27th and 39th order in UPDPWM with Sinusoidal reference and 5th, 27th, and 39th of Trapezoidal reference. b) 31st, 33rd, 37th and 39th in UAPODPWM with Sinusoidal reference and 5th, 31st, 33rd, 37th and 39th of Trapezoidal reference. c) 3rd, 5th, 37th and 39th in UCOPWM with Sinusoidal reference and 5th, 37th and 39th of Trapezoidal reference.

TABLE I

% THD FOR DIFFERENT MODULATION INDICES

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	17.97	15.27	18.22	15.71	22.92	21.02
0.95	20.41	19.04	20.15	19.04	25.14	23.52
0.9	22.09	21.54	22.05	21.11	27.59	25.94
0.85	23.40	23.52	23.18	23.40	29.71	28.9
0.8	24.19	24.60	24.12	24.82	32.39	30.37

TABLE II

V_{RMS} FOR DIFFERENT MODULATION INDICES

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	212.1	178.6	212.1	178.4	218.1	188.9
0.95	201.2	189.5	201.6	189.5	209.5	198.2
0.9	191.2	200.6	190.9	200.6	199.9	208
0.85	180.6	212	180.4	211.8	190.2	217.1
0.8	169.8	223.4	169.8	223	179.9	225.7

TABLE III

CREST FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	1.414427	1.5005599	1.414427	1.4142377	1.41403	1.4139756
0.95	1.414513	1.4970976	1.414187	1.4137203	1.413842	1.4142281
0.9	1.413703	1.4945165	1.414353	1.4142572	1.413707	1.4139423
0.85	1.414175	1.4900943	1.41408	1.4140699	1.414301	1.4140949
0.8	1.414016	1.4140555	1.414016	1.4143498	1.414119	1.4138237

TABLE IV

DISTORTION FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	0.000152862	0.00176742	0.00011	0.00174838	0.001994	0.00306268
0.95	0.000158236	0.00173392	0.000153	0.00175944	0.002409	0.00340048
0.9	0.000352789	0.00156423	0.000112	0.00168987	0.003612	0.00435418
0.85	0.000495208	0.00163992	0.00014	0.00169201	0.005506	0.00566812
0.8	0.000222905	0.00180185	0.000417	0.001695097	0.007018	0.00692015

TABLE V

FORM FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	65972.006	1631.0502	62235.915	109447.85	4234.9515	2733.3237
0.95	69093.407	84787.472	69661.368	73735.409	45652.648	53208.054
0.9	79073.615	4647.8221	86301.989	83933.054	52412.166	46211.953
0.85	107244.66	1843.4783	108413.46	2285.5293	62238.22	7073.9655
0.8	136166.8	5402.6602	136604.99	4527.9188	77409.639	3107.5313

VI. Conclusion

In this paper, UPWM techniques for new breed of asymmetrical DC source seven level inverter have been presented. New breed of unequal DC source multilevel inverter gives higher output voltage with reduced switch count and low harmonics. Performance factors like %THD, V_{RMS}, CF, FF and % DF have been evaluated presented and analyzed. It is found that the UPDPWM and UAPODPWM strategy with trapezoidal reference provides relatively lower %THD, UCOPWM strategy with trapezoidal reference is found to perform better since it provides relatively higher fundamental RMS output voltage.

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S.P.Natarajan was born in 1955 in Chidambaram. He has obtained B.E (Electrical and Electronics) and M.E (Power Systems) degrees in 1978 and 1984 respectively from Annamalai University securing distinction and then Ph.D in Power Electronics from Anna University, Chennai in 2003. He is currently Professor and Head of Instrumentation Engineering Department at Annamalai University where he has put in 33 years of service. He produced eight Ph.Ds and presently guiding eight Ph.D Scholars and so far guided eighty M.E students. His research papers 66 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 25 publications in national journals and 70 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of permanent magnet brushless DC motor, embedded control for multilevel inverters and matrix converters etc. He is a life member of Instrument Society of India and Indian Society for Technical Education.